

DP83903 Configurable Multiple Function PCMCIA Interface Chip

General Description

National's DP83903 acts as a standard interface between the PCMCIA bus and card-side local bus for I/O and memory PCMCIA cards. This device allows the card designer to focus on the design of the dual I/O functions while providing a one-chip solution for I/O memory window control, concurrent interrupt control, EEPROM interfacing, and power management. In addition to being configurable to interface to any two ISA compatible I/O functions, the DP83903 supports logic necessary to simplify a design that uses the National DP83902A ST-NIC Ethernet® Controller as one of the functions.

The DP83903 is fully compliant with PCMCIA version 2.1 and is compatible with serial 4-kbit and 16-kbit EEPROMs with 8-bit and 16-bit organizations that use the MICRO-WIRE™ protocol. This multi-function interface IC allows the system software to setup I/O decode windows and provides the Attribute memory decode control that allow attribute read and write data transfers.

Features

- PCMCIA Bus Interface
- Compliant with multi-function extension to PCMCIA Standards 3.X
- PCMCIA version 2.1 configuration registers
- Serial EEPROM interface compatible with MICROWIRE EEPROM protocol
- 2-kbyte on chip RAM for attribute memory which shadows the CIS and is used for loading static registers
- Address decoding and control for 2 I/O functions
- Logic to support any two interrupt capable I/O functions on a PCMCIA card
- Power management and clock control
- Programmable arbitration unit for PCMCIA host and two functions
- Common memory logic
- National DP83902A Ethernet LAN support logic for shared memory architecture only
- 4 Bit, direction programmable, generic digital port
- ISA-like interface to card function

1.0 System Diagram

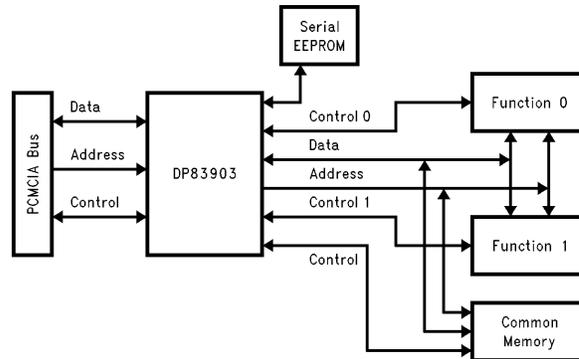


FIGURE 1-1

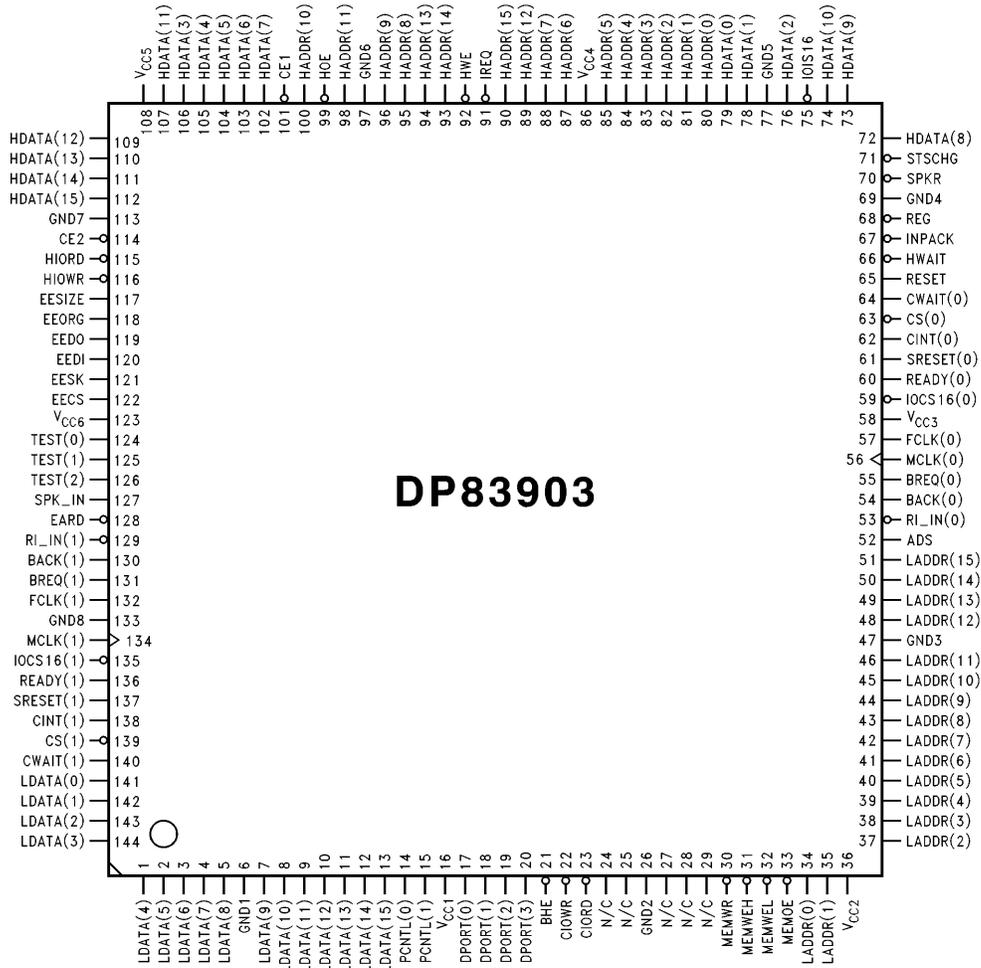
TL/F/12483-1

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Table of Contents

GENERAL DESCRIPTION AND PRODUCT FEATURES	1
1.0 SYSTEM DIAGRAM	1
2.0 CONNECTION DIAGRAM	3
3.0 PINOUT DESCRIPTION AND DETAILED TABLES	4
4.0 BLOCK DIAGRAM	7
5.0 FUNCTIONAL DESCRIPTION	8
5.1 Address Maps	8
5.1.1 Attribute Memory Addressing	8
5.1.2 I/O Memory Addressing	9
5.1.3 Common Memory Addressing	9
5.2 Registers	9
5.2.1 PCMCIA Registers	9
5.2.2 DP83903 Specific Registers	10
5.2.3 PCMCIA Standard Compliant Registers	10
5.2.4 LAN (National ST-NIC) Mode Register Set	14
5.3 Logic Descriptions	17
5.3.1 I/O Card Interface Logic for PCMCIA Host I/O Accesses	17
5.3.2 EEPROM Interface	17
5.3.2.1 CIS Data Security	18
5.3.3 Power Management	18
5.3.4 Bus Arbitration	19
5.3.5 Common Memory Management	19
6.0 OPERATIONAL MODES	19
6.1 Initial Setup (reset) and Configuration	19
6.2 Reset Conditions	19
6.3 Interrupt Control	19
6.4 Functional Concurrency	20
6.5 16-Bit/8-Bit Operation	20
6.6 Special Testability Modes	20
SOFTWARE	20
ABSOLUTE MAXIMUM RATINGS	22
RECOMMENDED OPERATING CONDITIONS	22
RELIABILITY REQUIREMENTS	22
DC ELECTRICAL CHARACTERISTICS	22
TYPICAL APPLICATIONS	38
REFERENCES	38

2.0 Connection Diagram



TL/F/12483-2

Order Number DP83903CS
See NSC Package Number VNG144A

3.0 Pinout Description

TABLE 3-1. PCMCIA Host-Side Pins

Pin Name	Pin Type	Pin No.	Level Compatibility	Internal Resistor	Description
HDATA(15:0)	I/O	112–109, 107, 74–72, 102–106, 76, 78, 79	TTL 6 mA	> 100k to GND	PCMCIA Host Data Bus.
HADDR(15:0)	I	90, 93, 94, 89, 98, 100, 96, 95, 88, 87, 85–80	TTL	> 100k to GND	PCMCIA Host Address Bus.
HOE #	I	99	TTL	> 100k to V _{CC}	PCMCIA Host uses this pin to read common or attribute memory space.
HWE #	I	92	TTL	> 100k to V _{CC}	PCMCIA Host uses this pin to write common or attribute memory space.
HIORD #	I	115	TTL	> 100k to V _{CC}	PCMCIA Host uses this pin to read I/O memory space.
HIOWR #	I	116	TTL	> 100k to V _{CC}	PCMCIA Host uses this pin to write I/O memory space.
IREQ #	O	91	CMOS 6 mA		Interrupt Request signal to PCMCIA Host.
HWAIT #	O	66	CMOS 6 mA		This pin allows the DP83903 to insert wait states in a PCMCIA transaction.
IOIS16 #	O	75	CMOS 6 mA		Low indicates this I/O access to the card is capable of 16-bit access. Function 0 and 1 may use their IOCS16(1:0) # respectively to control this signal and inform the host if a 16-bit access to the target is feasible.
INPACK #	O	67	CMOS 6 mA		Signals a valid I/O read.
CE1 #	I	101	TTL	> 100k to V _{CC}	Indicates even address byte. Odd addresses are not released. CE1 # and CE2 # assertion encodings are specified by the PCMCIA Specification.
CE2 #	I	114	TTL	> 100k to V _{CC}	Indicates odd addressing only. CE1 # and CE2 # assertion encodings are specified by the PCMCIA Specification.
REG #	I	68	TTL	> 100k to V _{CC}	Indicates access to attribute memory space or I/O address space. REG # must be high to access common memory space.
RESET	I	65	TTL Schmitt	> 100k to V _{CC}	Asynchronously resets the DP83903.
SPKR #	O	70	CMOS 6 mA		If Audio bits are set in the Card Configuration Status Register and in either of the Function Configuration Status Registers 0,1, then SPKR # is invert of SPK_IN pin, else SPKR # is high.
STSCHG #	O	71	CMOS 6 mA		STSCHG # is asserted when the Changed bit and SigChg bit are set in the Card Configuration Status Register.

3.0 Pinout Description (Continued)

TABLE 3-2. Serial EEPROM Interface Pins

Pin Name	Pin Type	Pin No.	Level Compatibility	Internal Resistor	Description
EEDO	I	119	TTL		Serial Data in from EEPROM.
EEDI	O	120	CMOS 6 mA		Serial Data out to EEPROM.
EECS	O	122	CMOS 6 mA		EEPROM Chip Select.
EESK	O	121	CMOS 6 mA		EEPROM Clock. Freq = MCLK(0)/32.
EESize	I	117	TTL	> 100k to V _{CC}	EEPROM Size. If high, the EEPROM size is 16-kbit, else the size is 4-kbit.
EEORG	I	118	TTL	> 100k to V _{CC}	EEPROM Organization pin. If high, the EEPROM is organized as 16-bit words, else organization is 8 bits.

Note: The Enable EEPROM function is performed in software by writing to the EEPROM Control Register. The Enable EEPROM bit will default to low (disabled) upon power on.

TABLE 3-3. Card-Side Interface Pins

Pin Name	Pin Type	Pin No.	Level Compatibility	Internal Resistor	Description
LDATA(15:0)	I/O	13–7, 5–1, 144–141	TTL 6 mA	Hold Circuit (Note 1)	Card-side Data Bus.
DPORT(3:0)	I/O	20, 19, 18, 17	TTL 6 mA		Generic, Direction programmable function port for additional user signals. In LAN Mode, these signals are assigned specific meaning for use with an Ethernet LAN IC.
EARD#	O	128	CMOS 6 mA		Chip select for external attribute memory not shadowed in DP83903 IC.
SPK_IN	I	127	TTL Schmitt		Input Audio Signal.
RI_IN(0)#	I	53	TTL Schmitt		Ring Indicator for function 0. In LAN Mode, this is a packet indicator input.
RI_IN(1)#	I	129	TTL Schmitt		Ring Indicator for function 1.
CIORD#	O	23	CMOS 6 mA		I/O read signals are passed through from HIORD# according to the expression shown below when a valid address is decoded. $CIORD\# = HIORD\# + REG\# + (CE1\# * CE2\#)$
CIOWR#	O	22	CMOS 6 mA		I/O write signals are passed through from HIOWR# according to the expression shown below when a valid address is decoded. $CIOWR\# = HIOWR\# + REG\# + (CE1\# * CE2\#)$
CWAIT(1:0)	I	140, 64	TTL		Card-side transaction wait state inputs.
CS(1:0)#	O	139, 63	CMOS 6 mA		Chip select for each function.
BHE#	O	21	CMOS 6 mA		Byte high enable. When de-asserted and CS()# asserted, an 8-bit access on LDATA(7:0) is in progress. This holds for both odd and even addresses. When asserted and CS()# asserted, a 16-bit access on LDATA(15:0) is in progress.
READY(1:0)	I	136, 60	TTL	> 100k to V _{CC}	Indicates that the function is either READY or ~READY (i.e. - Busy). This signal is used to assert the Rdy/Bsy# bit in Pin Replacement Registers.
CINT(1:0)	I	138, 62	TTL Schmitt		Card-side interrupt input signals.
SRESET(1:0)	O	137, 61	CMOS 6 mA		Signals reset to Card-side functions.

3.0 Pinout Description (Continued)

TABLE 3-3. Card-Side Interface Pins (Continued)

Pin Name	Pin Type	Pin No.	Level Compatibility	Internal Resistor	Description
IOCS16(1:0)#	I	135, 59	TTL		This pin is asserted during an access to a function if that function is capable of a 16-bit access.
BREQ(1:0)	I	131, 55	TTL		Bus requests for local DMA. (Remote DMA is not supported on current revision.)
BACK(1:0)	O	130, 54	CMOS 6 mA		Bus grants for local DMA. (Remote DMA is not supported on current revision.)
LA(15:0)	O Tri	51–48, 46–37, 35, 34	CMOS 6 mA	Hold Circuit (Note 1)	Local Address Bus. This may be equivalent to the HADDR(15:0) bus for PCMCIA Host reads/writes or a latched address from a DMA controller such as a LAN controller.
ADS	I	52	TTL		Address Strobe to latch LDATA(15:0) onto LA(15:0).
PCNTL(1:0)	O	15, 14	CMOS 6 mA		Power management control signals or general outputs.
MCLK(1:0)	I	134, 56	TTL Schmitt		Input clocks for function 0 and function 1.
FCLK(1:0)	O	132, 57	CMOS 6 mA		Output clock signals for function 0 and function 1. These may be gated on/off or be a divided value of MCLK(1:0).
MEMWR#	I	30	TTL	> 100k to V _{CC}	Common Memory write input for one function.
MEMWEH#	O Tri	31	CMOS 6 mA	> 10k to V _{CC}	Common Memory write output for upper byte of data word.
MEMWEL#	O Tri	32	CMOS 6 mA	> 10k to V _{CC}	Common Memory write output for lower byte of data word.
MEMOE#	O Tri	33	CMOS 6 mA	> 10k to V _{CC}	Common Memory read signal.
N/C		24, 25 27–29			No connect.

Note 1: The Hold Circuit will hold the signal to the logic value it was last set to when the line is TRI-STATE®. This will insure that inputs do not float during a TRI-STATE condition.

TABLE 3-4. Miscellaneous Pins

Pin Name	Pin Type	Pin No.	Level Compatibility	Internal Resistor	Description
TEST(2:0)	I	126, 125, 124	TTL	> 100k to GND	Test pins. These pins should be left disconnected for normal operation.
V _{CC} (5:0)	Power	16, 36, 58, 86, 108, 123			Power Voltage.
GND(7:0)	Power	6, 26, 47, 69, 77, 97, 113, 133			Return Voltage.

3.0 Pinout Description (Continued)

Pin Total:	
Host-Side Interface Pins	46
EEPROM Interface Pins	6
Card-Side Interface Pins	75
Miscellaneous Pins	17
Total Pins	144

4.0 Block Diagram

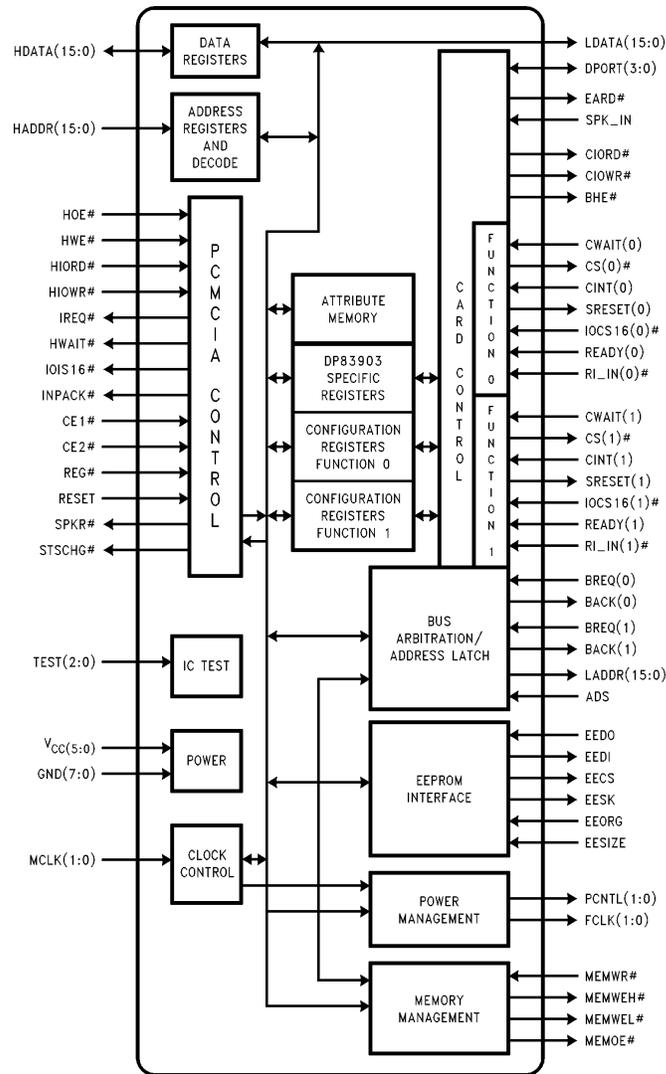


FIGURE 4-1

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5.0 Functional Description

The Multi-function PCMCIA card interface IC (integrated circuit) provides an integrated solution to interfacing dual function I/O cards with the PCMCIA Bus. The part has a contiguous 2-kbyte RAM block to store attribute memory. The IC also provides an EEPROM interface to serial EEPROMs that use the MICROWIRE protocol. At a minimum, a 4-kbit serial EEPROM is required. The 16-kbit EEPROM is optional. The part allows I/O address windows to be programmed independently for each function.

5.1 ADDRESS MAPS

5.1.1 Attribute Memory Addressing

The Attribute Memory space contains both the Card Information Structure (CIS), PCMCIA Registers for both functions, and DP83903 implementation specific registers. Note that PCMCIA specifies that Attribute memory may only be accessed on even address byte boundaries. The Attribute Memory space fragmentation is shown in Table 5-1.

TABLE 5-1. Attribute Memory Map

Register Description	Register Type	Address (Hex)	EEPROM
Card Information Structure	PCMCIA CIS	0x000-0x03E2	Yes
Pin Polarity Register	DP83903 Specific	0x03E4	Yes
PMGR and Clock Register	DP83903 Specific	0x03E6	Yes
CTERM 0 Register	DP83903 Specific	0x03E8	Yes
CTERM 1 Register	DP83903 Specific	0x03EA	Yes
Arbiter Priority Register	DP83903 Specific	0x03EC	Yes
Arbiter Latency Register	DP83903 Specific	0x03EE	Yes
Miscellaneous Register	DP83903 Specific	0x03F0	Yes
Digital Port Direction Register	DP83903 Specific	0x03F2	Yes
Digital Port Register	DP83903 Specific	0x03F4	Yes
Wait State Timer Register	DP83903 Specific	0x03F6	Yes
Reserved for Future Use Registers	DP83903 Specific	0x03F8-0x03FE	Yes
Card Information Structure	PCMCIA CIS	0x0400-0x0FFE	Optional
ID Register	DP83903 Specific	0x1000	No
EEPROM Control Register	DP83903 Specific	0x1002	No
Reserved for Future Use Registers	DP83903 Specific	0x1004-0x101E	No
Function 0 Configuration Option Register	PCMCIA	0x1020	No
Function 0 Configuration Status Register	PCMCIA	0x1022	No
Function 0 Pin Replacement Register	PCMCIA	0x1024	No
Unused	PCMCIA	0x1026	No
Function 0 I/O Event Register	PCMCIA	0x1028	No
Function 0 Base A Register	PCMCIA Extension	0x102A	No
Function 0 Base B Register	PCMCIA Extension	0x102C	No
Unused	PCMCIA Extension	0x102E-0x1030	No
Function 0 Limit Register	PCMCIA Extension	0x1032	No
Reserved for Future Use Registers	PCMCIA Extension	0x1034-0x103E	No
Function 1 Configuration Option Register	PCMCIA	0x1040	No
Function 1 Configuration Status Register	PCMCIA	0x1042	No
Function 1 Pin Replacement Register	PCMCIA	0x1044	No
Unused	PCMCIA	0x1046	No
Function 1 I/O Event Register	PCMCIA	0x1048	No
Function 1 Base A Register	PCMCIA Extension	0x104A	No

5.0 Functional Description (Continued)

TABLE 5-1. Attribute Memory Map (Continued)

Register Description	Register Type	Address (Hex)	EEPROM
Function 1 Base B Register	PCMCIA Extension	0x104C	No
Unused	PCMCIA Extension	0x104E–0x1050	No
Function 1 Limit Register	PCMCIA Extension	0x1052	No
Reserved for Future Use Registers	PCMCIA Extension	0x1054–0x105E	No

5.1.2 I/O Memory Addressing

National's DP83903 uses a pair of address base and limit registers to fragment the I/O Address space. This allows I/O transactions from the PCMCIA Host to be steered to the appropriate function.

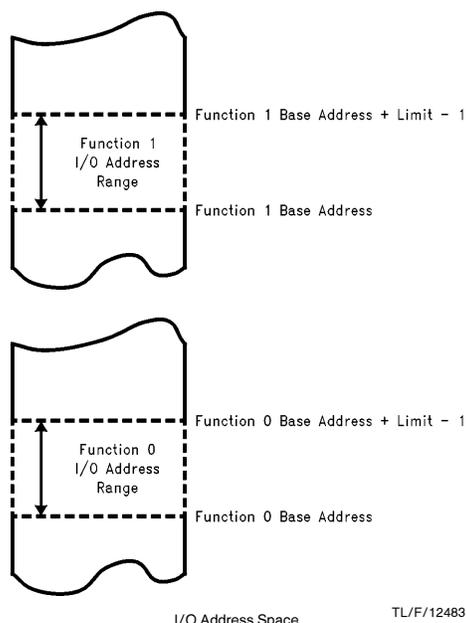


FIGURE 5-1. I/O Address Decoding for two functions on a PCMCIA Card

5.1.3 Common Memory Addressing

National's DP83903 does not specifically decode common memory address accesses initiated by the host. Rather, it will pass host accesses HADDR(15:0) through to LADDR(15:0) and HDATA(15:0) through to LDATA(15:0) once the host is granted access to the card using the arbiter. In addition, the DP83903 will pass the HOE# signal assertion through to the MEMOE# signal and the host HWE# signal assertion to the MEMWEH#/MEMWEL# signals appropriately. The assertion of MEMWEH#, MEMWEL#, or both is determined by an 8-bit or 16-bit access

and the address boundary as specified in the PCMCIA Specification. The functions are free to use common memory by arbitrating for the card local bus. If granted, the DP83903 will relinquish the LADDR(15:0) and LDATA(15:0) bus to the function.

If a function is mapped to common memory, such as a FLASH device, and requires further address lines, it may use the HADDR(25:16) lines from the PCMCIA socket as appropriate even though these signals do not go into the DP83903. These signals can be considered to be sideband to the DP83903. The card design is free to use external decoding logic for common memory.

For an Ethernet LAN card that desires to have a FLASH device, HADDR(16) may be used to fragment the Common Memory space into 2 pieces. When HADDR(16) is zero (0), the LAN SRAM buffers (up to 64-kbyte max) may be selected. When HADDR(16) is one (1), a 64-kbyte FLASH device may be selected. This use of one address line does not require an additional IC. If a FLASH device greater than 64k is desired, minimal decoding logic would become necessary.

5.2 REGISTERS

5.2.1 PCMCIA Registers

The PCMCIA register's context is for its respective function. Each function (0,1) has its own set of Configuration Registers so that each function may be configured and operated on independently from a programming model viewpoint.

CIS (CARD INFORMATION STRUCTURE)

[0x000–0x03E2]

When the DP83903 powers on, the contents of the lower 2.0/0.5-kbyte of the EEPROM are loaded into the device's shadow RAM. This not only allows attribute memory accesses to the CIS, but, it also provides defaults for 10 DP83903 specific registers to be loaded. This allows default loading of parameters that are transparent to system or device software. The best use is for the card manufacturer to determine what values these should be and program them into the EEPROM when the CIS is programmed. Either system software such as Card Services/Socket Services or device software may read and parse the CIS by accessing attribute memory on the PC Card. If desired, this software agent may write to the CIS or default EEPROM registers and, if desired, have these new values saved to the EEPROM. The actual contents of the CIS and the static registers is PC Card design dependent.

5.0 Functional Description (Continued)

5.2.2 DP83903 Specific Registers

These registers are defined specifically for National's DP83903 IC and are not part of the PCMCIA specification. These registers allow the DP83903 IC to perform its base functionality of supporting two general functions on a PC Card.

Pin Polarity Register [0x03E4]

This register sets the polarity of the card side interface signals.

D7	D6	D5	D4	D3	D2	D1	D0
CLOWR	CIORD	SRESET1	SRESET0	BHE	MemIs8	CWAIT1	CWAIT0

CLOWR, CIORD—Sets the polarity of the CLOWR# and CIORD# pins respectively. A high indicates active high. The default polarity is active-low.

SRESET1, SRESET0—Sets the polarity of the SRESET(1) and SRESET(0) pins respectively. When this bit is set to a zero (0), the output signal is asserted in the high (1) state. When this bit is set to a one (1), the output signal is asserted in the low (0) state. The bit default is zero (0), i.e. the SRESET() signal is active high.

BHE—Sets the polarity of the BHE# pin. A high indicates active-high. The default polarity is active-low.

MemIs8—This bit is set to one (1) if common memory is organized for 8-bit access. This bit is set to zero (0) if common memory is organized for 16-bit access. The default value is zero (0). This information allows the DP83903 to properly access memory using the MEMWEH#, MEMWEL#, and MEMOE# signals.

CWAIT1, CAWAIT0—When this bit is set to one (1), the DP83903 interprets this input signal active when it is low (0). When this bit is set to zero (0), the DP83903 interprets this input signal as active when it is high (1). The default bit value is zero (0), i.e. the CAWAIT() input signal is asserted high (1).

PMGR and Clock Register [0x03E6]

The Power Manager (PMGR) and Clock Register is used for controlling the PCNTL(1:0) pins for either power management purposes or general purpose digital output only. Unlike the Digital Port Register, there is no associated direction register since only outputs are allowed.

Hardware power management is enabled using the Function Configuration Option Register's Function Configuration Index values. Its use is intended for functions that can be sequenced on/off or into idle or sleep states with a quick (< 10 μ s) response time when powered on again. That is, the function may use its CAWAIT() signal to extend a transaction that caused the DP83903 to turn it on. Use of the READY() signal in a dynamic hardware power managed environment to set the RRdy/Bsy bits in order to achieve > 10 μ s response times for power on is not guaranteed to work since system software may not inspect the RRdy/Bsy bit in all such instances.

D7	D6	D5	D4	D3	D2	D1	D0
F1CLKEN	DIV1	PPOL1	PCNTL(1)	F0CLKEN	DIV0	PPOL0	PCNTL(0)

F1CLKEN, F0CLKEN—If set, these enable the pins FCLK(1:0) to receive a clock out. If clear, the respective pins FCLK(1:0) will be forced low. These are set and cleared by software if desired or statically loaded upon card power up from the EEPROM.

DIV1, DIV0—If set, the respective clock output from FCLK(1:0) will be divided by 32 from the input clocks MCLK(1:0). If clear, the clock output FCLK(1:0) will equal the respective clock input MCLK(1:0). These are set and cleared by software if desired or statically loaded upon card power up from the EEPROM.

PPOL1, PPOL0—Sets the active polarity of the PCNTL(1) and PCNTL(0) signals such that the function is asserted. If PPOL is set to zero (0), PCNTL() is asserted when in the high state. If set to one (1), PCNTL() is asserted when in the low state. The default is set to zero (0), i.e. PCNTL() defaults to active high.

PCNTL(1), PCNTL(0)—These bits control the pins PCNTL(1) and PCNTL(0) respectively. If hardware power management is not selected in the Function Configuration Option Register's Function Configuration Index, then these bits may be used as output signals by software for general purposes. If the hardware power management configuration is selected, these bits are de-asserted (defined by PPOL1, 0) when the DP83903's CTERM 1 or 0 counter expires. These bits will be asserted if a transaction occurs to the function through an I/O window, the function requests the card-side bus using BREQ() or the function issues a RL_IN(). In either strategy, software may always write and read back these bits. These bits default to zero (0) during power-on until the PMGR and Clock Register can be loaded from the EEPROM.

CTERM Registers 0, 1 [0x03E8, 0x03EA]

These registers are used to define the value of function 0's and function 1's power time-out counters respectively. If a function's power time-out counter expires, the PCNTL bit for that function in the PMGR and Clock Register is de-asserted. This will occur if a function is in-active long enough for its power time-out counter to expire. Active is defined as having either an I/O access from the host, receiving a BREQ() or a RL_IN()#. Devices that may operate for long periods of time without a host I/O access and do not use BREQ() should follow a software controlled power management strategy that uses the PwrDn bits in the Function Configuration Status Registers 0, 1.

D7-D0
N = Time-Out Counter Terminal Count Value

Each function's terminal counter is 8 bits wide and counts at a rate of MCLK(0)/(2¹⁷). For example, if the MCLK(0) frequency is 30 MHz the device can be programmed to time-out between 0.0s to 1.114s. The general formula is:

$$\text{Time} = (1/\text{mclk}(0)) * 2^{17} * N,$$

where N = {0, 1, 2, . . . , 255}

For a 5 MHz MCLK(0) frequency, the equation is:

$$\text{Time} = N (26.2144 \text{ ms}) \text{ where } N = \{0, 1, 2, \dots, 255\}$$

Note: A value of zero implies the function is powered down.

5.0 Functional Description (Continued)

Arbiter Priority Register [0x03EC]

This register controls the priority (from the set {00,01,10,11}) for each possible card-bus master from the set {PCMCIA Host, Function 0, Function 1}. The value of {3} is the highest priority whereas {0} is the lowest priority.

D7	D6	D5-D4	D3-D2	D1-D0
ArbiterCLK	PreemptEnb	PCMCIA Host Priority	Function 1 Priority	Function 0 Priority

ArbiterCLK—This bit is set to one (1) to increment the Arbiter Latency Register using $MCLK(0)/16$. This bit is set to zero (0) to increment the Arbiter Latency Register using $MCLK(0)/1$.

PreemptEnb—If this bit is set to one (1), the arbiter will allow pre-emption of bus masters. If this bit is set to zero (0), the arbiter will allow a bus master to complete before granting the bus to another master as determined by the priority scheme used.

Arbiter Latency Register [0x03EE]

This register programs a latency timer such that when a card-bus master is in control of the bus and another unit requests and wins access to the bus (following priority scheme), the timer will allow the current bus owner to retain the bus until the timer expires. This is useful when pre-emptions are allowed using the PreemptEnb bit in the Arbiter Priority Register. The timer does not start counting down until the arbiter queues another device for bus ownership.

D7-D0
N = Arbiter Latency Timer Value

Arbiter Latency Timer Value (N)—This value is used by an arbiter counter. Therefore, the latency time until the $BREQ()$ is relinquished (or internal host $BREQ$) when PreemptEnb is set to one (1) is:

Latency Time = $16(N)/f_{MCLK(0)}$ when ArbiterCLK = (1)

Latency Time = $(N)/f_{MCLK(0)}$ when ArbiterCLK = (0)

Miscellaneous Register [0x03F0]

D7	D6	D5	D4-D0
FastEE	LA_TRI_Func1	LA_TRI_Func0	EEPROMStartAddr

FastEE—If this bit is set to one (1), then the clock used to access the EEPROM shall be $MCLK(0)/2$. If this bit is set to zero (0), the clock used to access the EEPROM shall be $MCLK(0)/32$.

LA_TRI_Func1, LA_TRI_Func0—This bit should be set to one (1) when a bus master function will multiplex address and data on the $LDATA()$ bus and will use ADS to strobe the address phase on this bus to the $LADDR()$ bus. In this case, the DP83903 will drive the $LADDR()$ bus and latch the $LDATA()$ bus to the $LADDR()$ bus on an ADS strobe. This bit should be set to a zero (0) when a bus master function will drive the $LADDR()$ bus directly. In this case, the DP83903 will TRI-STATE (not drive) the $LADDR()$ bus when it is granted to function 0 or function 1 in expectation that the function will control the $LADDR()$ bus.

EEPROMStartAddr—This field contains a starting address for EEPROM read or write access. This is ordinarily set to zero and is used for debug/test purposes.

Digital Port Direction Register [0x03F2]

This register is a read/write register that controls the direction for each individual bit in the Digital Port Register.

D7-D4	D3	D2	D1	D0
Reserved	DPDIR3	DPDIR2	DPDIR1	DPDIR0

DPDIR3,2,1,0—DPDIRi defines the direction of the corresponding DPORT(i) pin and, hence, the direction of the DPORTi bit in the Digital Port Register. If DPDIRi is set to zero (0)(default), then the DPORT(i) pin is a digital input. If DPDIRi is set to one (1), then the DPORT(i) pin is a digital output.

Digital Port Register [0x03F4]

The Digital Port Register is a read/write register connected to the DPORT(3:0) pins of the DP83903 chip. Each bit is direction programmable through software using the Digital Port Direction Register.

D7-D4	D3	D2	D1	D0
Reserved	DPORT3	DPORT2	DPORT1	DPORT0

DPORT3,2,1,0—If DPDIR is set to one (1) then DPORT may be written to. The value written will be sourced by the corresponding DPORT pin. When DPORT is read, the value returned will be the last value written to DPORT. If DPDIR is reset to zero (0) then DPORT will assume the value externally driven into the corresponding DPORT pin. Therefore, when DPORT is read, it returns the value being driven into the DPORT pin. When written, the value is unaffected and retains the value driven on DPORT.

Wait State Timer Register [0x03F6]

This register allows the insertion of default wait states from the DP83903 using $HWAIT\#$. It is intended to be used in situations where either the function is too slow to respond with a $CWAIT()$ or the unique wait timing constraints between the system and PC Card design necessitate a default wait state.

D7-D4	D3-D2	D1-D0
Reserved	Func1Wait	Func0Wait

Func1Wait, Func0Wait—This value is the number (0, 1, 2, or 3) of $MCLK(0)$ time periods that the DP83903 will assert $HWAIT\#$ during a valid access to a particular function. For Zero wait states, program these values to 00b.

ID Register [0x1000]

This read only register provides the software with IC revision information.

D7-D3	D2-D0
DP83903 Code = 00000b	Revision Code = 001b

National DP83903 Code—This code may be used to identify the DP83903 IC. The value of this register is 00000b.

Revision Code—This will uniquely identify the silicon version of the device.

5.0 Functional Description (Continued)

EEPROM Control Register [0x1002]

This register controls reading and writing the EEPROM as well as the EEPROM enable.

D7	D6	D5-D1	D0
WriteEEPROM	ReadEEPROM	Reserved	Enable EEPROM

WriteEEPROM—When set, this tells the EEPROM controller to copy the contents of the DP83903 Shadow RAM to the EEPROM. Once done, the EEPROM controller clears this bit.

ReadEEPROM—When set, this tells the EEPROM controller to copy the contents of the EEPROM to the shadow RAM. Once done, the EEPROM controller clears this bit. Any data modified in the Shadow RAM that has not first been written back to the EEPROM will be lost.

Enable EEPROM—This must be set to allow EEPROM writes. If clear, the EEPROM may not be written. The default value at reset is low. The EEPROM may be read independent of the value of this bit.

Note 1: Upon power-up, the DP83903 EEPROM controller copies the entire contents of the EEPROM (size dependent) into the Shadow RAM.

Note 2: The DP83903 EEPROM controller stores data in a 16-bit organized EEPROM in low/high format. Although Attribute Memory is on even byte boundaries only, the entire EEPROM's address space is used. This eliminates waste of EEPROM memory. Therefore the Attribute space used by the Shadow RAM is double the actual size of the EEPROM. For example, if a 16-bit EEPROM is pre-programmed, the low byte at word 0 in the EEPROM will be shadowed at Attribute location 0x0000 and the high byte will be shadowed at Attribute location 0x0002. The low byte at EEPROM word 1 will be shadowed to Attribute location 0x0004, etc. For EEPROM organizations of 8 bits, EEPROM byte 0 will be shadowed to Attribute location 0x0000 and byte 1 will be shadowed to Attribute location 0x0002.

5.2.3 PCMCIA Standard Compliant Registers

Function Configuration Option Registers 0,1

[0x1020,0x1040]

D7	D6	D5-D0
SRESET	LeviREQ	Function Configuration Index

SRESET—If the host sets this field to one (1), the DP83903 shall place the given function in the reset state. When the host returns this field to zero (0), the function shall enter the same unconfigured, reset state as it does following a power-up and hardware reset.

LeviREQ—When the DP83903 is being used as a PCMCIA I/O interface and this field is set to one (1), the DP83903 shall generate Level Mode interrupts for the function using the IREQ# signal. If the DP83903 is being used as a PCMCIA I/O interface and this field is set to zero (0), the DP83903 shall generate Pulse Mode interrupts for the function. Use of Level Mode interrupts for both functions when the DP83903 is configured for multi-function operation is strongly recommended. Since there is only one PCMCIA Bus interface, the LeviREQ bits for Function 0 Configuration Option Register and Function 1 Configuration Option Register are aliased. The DP83903 will also only allow a write to the LeviREQ bit value to change the interfaces Interrupt level mode if the given function is configured using ConfFunc and interrupts are enabled using EnbIREQ.

In addition, the DP83903 provides an enhanced interrupt protocol scheme described by the IntrReset bit in the Function Configuration Status Registers 0, 1. The DP83903 implements a shared interrupt scheme in multi-function operation. Single function configurations may use Level Mode or Pulse Mode interrupt schemes. Pulsed Mode interrupt width is given by:

$$TwidthIREQ = 16/(FreqMCLK(0))$$

Using MCLK(0) from 5 MHz–30 MHz will insure pulse widths from 0.53 μ s–3.2 μ s which exceed the 0.5 μ s minimum requirement for PCMCIA.

Function Configuration Index—When the host system sets this field to the value of the Configuration Entry Number field of a Configuration Table Entry Tuple, the function shall enter the configuration described by that tuple. This field shall be reset to zero (0) by the DP83903 when the host sets the SRESET field to one (1) or the host asserts RESET. If this field is set to zero (0) explicitly by the host or implicitly by SRESET or RESET, the function shall use the Memory Only interface and I/O cycles from the host shall be ignored by the function.

The following configurations are supported by the Function Configuration Index 0, 1:

ConfFunc (D0)—If this is set to one (1), then the Card is configured for that function.

EnbBase_Limit (D1)—If this is set to a one (1), the base and limit register pair for the function is enabled. That is, the DP83903 will only pass I/O transactions whose address falls within the I/O window specified by the base and limit pair. If this is set to a zero (0), the DP83903 will not test transactions' addresses against the base and limit pair for that function and will, therefore, pass all I/O transactions to the function. For single function operation, the EnbBase_Limit would be enabled for operation with host controllers that support overlapping windowing and the INPACK# signal. For host controllers that do not support INPACK# but are capable of windowing granularity required for the function, EnbBase_Limit may be set to zero (0) so that all I/O transactions are passed to the function. For multifunction operation, the EnbBase_Limit bits for both functions should be set to one (1).

EnbIREQ (D2)—When the DP83903 is being used as a PCMCIA I/O interface and this field is set to one (1), the DP83903 shall enable this function to interrupt the host using the IREQ# signal. Normally this bit would be set to one (1). In environments where the function's software driver will use a polling technique for status information, this bit could be set to zero (0) to disable interrupts from that function.

PMGMT_EN (D3)—This bit, if set to a one (1), enables the hardware power management controller to control the PCNTL() pin for that function. See the PMGR and Clock Register description.

LAN Mode (D4 for Function 0 Configuration Option Register only)—When this bit is set to a one (1), the Function 0 interface on the DP83903 will support National's DP83902A Ethernet LAN IC in shared memory mode only. Function 0 is said to be in LAN Mode.

5.0 Functional Description (Continued)

Function Configuration Status Registers 0,1

[0x1022,0x1042]

These PCMCIA registers are used for function control/status information.

D7	D6	D5	D4	D3	D2	D1	D0
Changed	SigChg	IOis8	Reserved	Audio	PwrDn	Intr	IntrReset

Changed—If one or more of the state change signals in the Function Pin Replacement Register are set to one (1), the DP83903 shall set this field to a one (1). If the DP83903 is being operated as a I/O interface, (PC Card using I/O Interface), and both the Changed and SigChg fields are set to one (1), the DP83903 shall assert the STSCHG# signal. If the PC Card, and hence DP83903, is not using the I/O interface, this field is undefined and ignored.

SigChg—This field serves as a gate for asserting the STSCHG signal. If the DP83903 is operated as an I/O interface, and both the Changed and SigChg fields are set to one (1), the DP83903 shall assert the PCMCIA STSCHG# signal. If the DP83903 is operated as an I/O interface and this field is reset to a zero (0), the DP83903 shall not assert the STSCHG# signal. If the DP83903 is not operated as an I/O interface, this field is undefined and should be ignored. Either Function Configuration Status Register 0 or 1 is capable of asserting STSCHG# if it satisfies the above requirements.

IOis8—When the host can only provide I/O cycles with an 8-bit D0–D7 path, the host shall set this bit to a one (1). The card is guaranteed that accesses to 16-bit registers will occur as two, byte accesses rather than a single 16-bit access. This information is useful when 16-bit and 8-bit registers overlap.

Audio—Sampling of the signal SPK_IN and control of SPKR# is accomplished using the Audio bit. SPKR# will equate to SPK_IN anytime either of the Audio bits is set to one (1) and the function is configured.

PwrDn—When the host sets this field to one (1), the DP83903 shall set the given function to a power-down state by de-asserting the PCNTL() signal for that function. While this field is a one (1), the host shall not access the function on the PC Card. The host shall return this field to zero (0) before attempting to access the function. The system shall not place the card into a power-down state while the card's RDY/BSY# line is in the low (Busy) state. All input/output signals particular to the function are TRI-STATE.

Intr—If the function is requesting interrupt servicing (CINT() asserted), the DP83903 shall set this field to one (1). The DP83903 shall reset this field to zero (0) when the interrupt request has been serviced (CINT() de-asserted).

IntrReset—If IntrReset is set to zero (0), Intr shall be set to one (1) when an interrupt condition occurs and shall be reset to zero (0) when the interrupt condition has been serviced. A write to the Intr bit will do nothing. If IntrReset is set to one (1), Intr shall be set to one (1) when an interrupt condition occurs (CINT() pin) and be cleared to a zero (0) when the interrupt (CINT() pin) is serviced, however, a write of value zero (0) to any FCSR's Intr bit where IntrReset is set to one (1) shall cause the DP83903 to evaluate all CINT() signals and generate another interrupt to the system if an interrupt is pending. Note that the write of zero (0) to any FCSR's Intr bit where IntrReset is set to one (1) is an indication to the DP83903 that it must evaluate all CINT()

pins and generate a specified pulse to the system on the IREQ line. This protocol will work in either pulse or level mode (state of aliased LevIREQ controlling IREQ# PCMCIA signal mode). Functions operate by asserting their CINT() signal when an interrupt condition occurs. If interrupts are enabled for a given function, then that function's CINT() pin, when asserted, may generate an interrupt within the DP83903.

National's DP83903 has access to an internal interrupt line that represents the OR of all interrupts that have been asserted and enabled. Since functions use a level mode interrupt approach, this OR'd internal interrupt signal represents a level mode ORing of the interrupts. When the OR'd signal is asserted, the DP83903 will generate either a pulse mode or level mode interrupt on the IREQ# line. Before EOI processing by the functions ISR, the function's interrupt condition will be cleared and its CINT() pin will de-assert. If no other interrupts are being asserted, the DP83903's internal line will de-assert IREQ#. If other interrupts are pending, the internal line remains asserted (and hence IREQ#). Since the standard PC compatible interrupt controller requires a positive edge to trigger an interrupt, system software based on using the IntrReset protocol for the DP83903 may write a zero (0) to any Intr bit where IntrReset is set to one (1) after EOI processing is done. This will cause the DP83903 to generate a pulse on the IREQ# line if any CINT() that's enabled is still asserted. In other words, if the internal line is still asserted at this point. If in pulse mode, this is a single pulse that goes high-low-high with at least 0.5 μ s low time. If in level mode, this pulse is a low-high-low pulse to trigger the interrupt controller and then remain low (IREQ# asserted) and be maintained low by the level mode interrupt. This protocol solves both the need for two positive edges during level mode interrupts when an interrupt occurs during an interrupt in-service and solves the need for separate-distinct pulse interrupts that do not overlap during two interrupt events close in time.

Note: For consistency, the DP83903 will alias all IntrReset bits on a write to insure that both functions operate in the same mode. Also, the Intr bits are aliased on writes as an indicator to the DP83903 that interrupt status must be checked and pulses generated per the above protocol.

Function Pin Replacement Registers 0,1

[0x1024,0x1044]

These PCMCIA registers replace the signals missing from a PCMCIA Memory Card interface due to using the PCMCIA I/O interface.

D7	D6	D5	D4	D3	D2	D1	D0
CBVD1	CBVD2	CRdy/Bsy	CWProt	RBVD1	RBVD2	RRdy/Bsy	RWProt

CBVD1, CBVD2—These bits are not implemented.

CRdy/Bsy—This bit is set to one (1) when RRdy/Bsy bit changes state.

CWProt—This bit is not implemented.

RBVD1, RBVD2, Rdy, Bsy, RWProt—Only RRdy/Bsy is implemented for each function. This bit reflects the state of the functions READY() input pin on the DP83903.

Note: The RRdy/Bsy bit (D1) follows the READY() inputs prior to the functions being configured.

5.0 Functional Description (Continued)

Function I/O Event Registers 0,1 [0x1028,0x1048]

D7-D6	D5	D4	D3-D2	D1	D0
Reserved	PIEvt	RIEvt	Reserved	PIEnab	RIEnab

PIEvt—In normal operation (not LAN Mode), the PIEvt bit is unused. In LAN Mode of operation, the PIEvt bit for Function I/O Event Register 0 is set to a one (1) if the $RI_IN(0)\#$ signal is asserted. The PIEvt bit for Function 1 I/O Event Register is unused.

RIEvt—In normal operation DP83903 latches a one (1) to the Card I/O Event Register's RIEvt bit when the $RI_IN(0)\#$ is set for the Function 0 I/O Event Register or when the $RI_IN(1)\#$ is set for Function 1 I/O Event Register. In LAN Mode of operation, the RIEvt bit for Function 0 I/O Event Register is unused.

Note: To clear PIEvt and RIEvt, bits 4 and 5, both bits must be written to simultaneously.

PIEnab—When this bit is set to a one (1), a latched value of one (1) on the PIEvt bit shall cause the Changed bit in the Function's Configuration Status Register to be set to a one (1).

RIEnab—When this bit is set to a one (1), a latched value of one (1) on the RIEvt bit shall cause the Changed bit in the Function's Configuration Status Register to be set to a one (1).

Function Base Address Registers 0,1 [0x102A-0x102C,0x104A-0x104C]

The base address for each function is comprised of 4 bytes (2 bytes implemented) that specify the base I/O address from which to begin decoding for chip selection of a particular function.

Base A Register

D7-D0
Byte 0 (Base Address bits 7-0) of 32-bit Address

This register comprises the low 8 bits of the base address for the Function I/O decode selection.

Base B Register

D7-D0
Byte 1 (Base Address bits 15-8) of 32-bit Address

This register comprises the next 8 bits of the base address for the Function I/O decode selection.

Base C Register

D7-D0
Byte 2 (Base Address bits 23-16) of 32-bit Address

This register is unused in the DP83903.

Base D Register

D7-D0
Byte 3 (Base Address bits 31-24) of 32-bit Address

This register is unused in the DP83903.

Using Base A and Base B Registers for each function supported by the DP83903 allows a 16 bit base address to be specified for I/O decoding and selection of function 0 and function 1 separately.

Function Limit Address Registers 0,1 [0x1032,0x1052]

The value placed in this register is a bit mask used to indicate which address bits the DP83903 will not decode. A value of one (1), indicates that the DP83903 will not decode the corresponding address line. A value of zero (0) indicates the DP83903 shall decode the corresponding address line. For proper operation, only contiguous sequences of ones (1) starting at bit 0 and moving leftward are allowed. For example, 00001001 is illegal whereas 00000111 is legal. This implies that the window size must be equal to a value of 2 raised to a integer power.

D7-D0
Limit Address Size

The following Limit Address Size values are legal and correspond to a particular I/O address decoding window size.

Limit Address Size Value	Window Size
0000 0000	NULL. Do not pass any I/O transactions to function unless base and limit checking is disabled in the function's COR.
0000 0001	2 bytes
0000 0011	4 bytes
0000 0111	8 bytes
0000 1111	16 bytes
0001 1111	32 bytes
0011 1111	64 bytes
0111 1111	128 bytes
1111 1111	256 bytes

Note: The window created using the Base Register in conjunction with the Limit Register is naturally aligned to the size of the window (as specified by the Limit Register) and not to the value programmed in the Base Register.

For example:

Base Register	Limit Register	Window Range	Aligned to Base
0374h	07h	0370h-0377h	No
03F8h	07h	03F8h-03FFh	Yes

5.2.4 LAN (National DP83902A) Mode Register Set

The LAN (National's DP83902A) Registers are only instantiated when the LAN Mode bit in the Function 0 Configuration Option Register is set to one (1). In LAN Mode, the Miscellaneous Status Register and the Reset Register support LAN functionality required within the DP83903. The LAN DP83902A feature also requires the DP83903 configuration registers to be set to the values shown in Table 5-2. This feature eases the use of existing National DP83902A software drivers and eliminates external glue logic. When in LAN Mode, a Remote DMA I/O Port and LDATA(15:0) to LADDR(15:0) latch mechanism is enabled for use by the DP83902A. The National DP83902A should be connected as function 0 on the PC Card and the use of the LAN registers is strongly recommended. Refer to *Figure 5-2* for DP83903 and DP83902A hardware connections.

5.0 Functional Description (Continued)

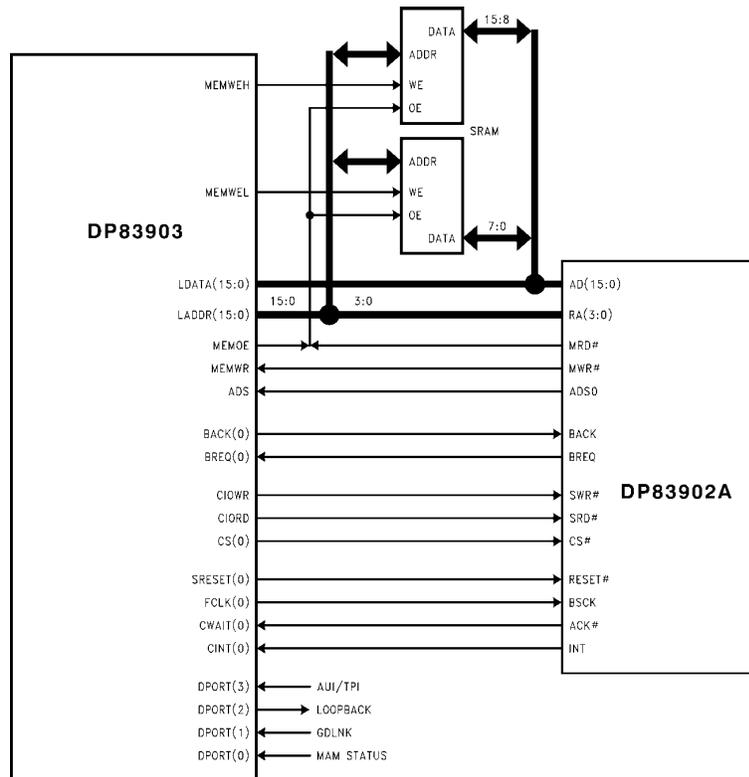


FIGURE 5-2. DP83903 and DP83902A Connection Schematic

TL/F/12483-12

Note: The FCLK(0) connection requires that MCLK(0) frequency is within the operating range of the DP83902A (typically 20 MHz). This schematic assumes that two 32k x 8 SRAMs are organized as shown to form a word-wide ring buffer and a 16-bit memory organization. For detailed pin descriptions refer to the NSC DP83902A datasheet.

TABLE 5-2. Configuring the DP83903 Register

Register Name	Register Offset (Hex)	Register Setting (Binary)	Comment
Pin Polarity Register	03E4	00X100X0	SRESET(0), CIOWR, CIORD, BHE active low; CWAIT(0) active high.
PMGR and FCLK	03E6	XXXX1001	FCLK(0) enabled; PCTL(0) on.
BUS ARB	03EC	0001XX00	Pre-empt off; host- priority 1; f0- priority 0.
MISC REG	03F0	0X1XXXXX	f0 Bus multiplexing enabled.
Configuration Option Reg 0	1020	01010111	f0 configured; Level IREQ; Base & limit enabled; IREQ enabled.

Note: The CIS structure for the LAN function must be written such that bit 4 of Configuration Option Register 0 is set to a 1 (LAN-Mode enabled) when function 0 is configured during card enabling. The register values programmed into registers 3e4-3f0 are stored in EEPROM, and will be configured at boot-up. Function 1 values are listed as don't care (X), their settings have no effect on function 0.

5.0 Functional Description (Continued)

DP83902A SHARED MEMORY MODE OPERATION

In the Shared Memory Mode, the DP83902A uses its local DMA controller to move data between itself and the local buffer SRAM. In this mode, the SRAM is memory mapped into the system's memory space. The Data I/O Register will not be used to transfer data. Rather, common memory accesses from the host system are required.

Packet Reception

- During reception, the DP83902A Local DMA Controller will request the LDATA(15:0) bus by asserting BREQ(0).
- The DP83903 will respond with BACK(0).
- The DP83902A places the appropriate SRAM Address on the LDATA(15:0) bus and then strobes ADS to latch the address on LADDR(15:0).
- The DP83902A places the data onto LDATA(15:0).
- The DP83902A issues a MEMWR# to the DP83903 which asserts MEMWEH# and MEMWEL# to the SRAM.
- The cycle ends when the DP83902A deasserts MEMWR#.
- This continues until the packet has been transferred into the SRAM.
- At the end of the packet reception, the DP83902A determines if the packet should be accepted or rejected and then issues an interrupt to the host through the DP83903.
- If accepted, the driver software operating on the host will transfer the packet data out of the SRAM to system memory. If not accepted, the error is recorded and the buffer space is recycled.

Packet Transmission

- The host transfers a packet from system memory to on-card SRAM.
- The host driver informs the DP83902A that a packet requires transmission.
- The DP83902A begins responding by requesting the bus using BREQ(0).
- The DP83903 asserts BACK(0) to the DP83902A.
- The DP83902A places an address on LDATA(15:0).
- The DP83902A latches this address to LADDR(15:0) by strobing ADS.
- The DP83902A issues MRD# to the SRAM and reads the SRAM data into the DP83902A FIFO. The FIFO data is serialized and transmitted over the network.
- This continues until the entire packet is transmitted over the network.

Miscellaneous Status Register

[I/O: Function 0 Base + 0x018]

This register is located at an I/O Address offset of 0x018h above the base address for function 0 when the LAN Mode bit is set to one (1) in the Function 0 Configuration Option Register. This register provides specific Ethernet LAN input

and output through the DPORT(3:0) pins and includes a HWAIT# time-out watchdog timer.

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Wait_Tout Enable	Reserved	Reserved	AUI/TPI	Loopback	GDLNK	Mam Status

Wait_Tout Enable—When this bit is set to a one (1), the HWAIT# time-out watchdog timer is enabled. In addition, the ability to set Intr in the Function Configuration Option Register 0, Intr in the Card Configuration Register, and IREQ# is enabled once the watchdog timer expires. The watchdog timer may expire if HWAIT# is asserted for more than approximately 11.2 μ s when MCLK(0) is set to 20 MHz for Ethernet LAN operation. This prevents the system from hanging due to prolonged HWAIT# assertions.

AUI/TPI—This read only bit is set to zero (0) if the Ethernet is in TPI Mode and set to one (1) if in AUI Mode.

Loopback—This write only bit is set to one (1) to perform DP83902A loopback mode testing. This bit is set to zero (0) otherwise.

GDLNK—This read only bit is only valid if in TPI mode (AUI/TPI is zero (0)). If reset to zero (0), the twisted pair link is good, if set to one (1), the twisted pair link fails.

Mam Status—This read only bit is set to zero (0) if no MAM is connected. The bit is set to one (1) if the MAM is connected (Twisted pair or Coax).

Note: The Miscellaneous Status Register bits 3 through 0 use the Digital Port Register bits 3 through 0 for physical connection to the AUI/TPI, Loopback, GDLNK, and Mam Status signals. When in LAN Mode, the Digital Port Direction Register (Attribute space) defaults to the following. It may not be read/written to in the attribute memory space when in LAN Mode.

D7-D4	D3	D2	D1	D0
Reserved	DPDIR3	DPDIR2	DPDIR1	DPDIR0
0	0 (Input)	1 (Output)	0 (Input)	0 (Input)

The Digital Port Register (Attribute space) should be connected as follows.

D7-D4	D3	D2	D1	D0
Reserved	DPORT3	DPORT2	DPORT1	DPORT0
No Pin Connections	Connect AUI/TPI to DPORT(3) pin	Connect Loopback to DPORT(2) pin	Connect GDLNK to DPORT(1) pin	Connect MAM Status to DPORT(0) pin

Reset Register

[I/O: Function 0 Base + 0x01F]

This read only register located at I/O Address offset 0x01Fh above the base address for function 0 is used to initiate a software reset to the DP83902A. When this register is read, the SRESET(0) (Note, in LAN Mode, the SRESET0 bit in the Pin Polarity Register should be programmed to one (1) to insure SRESET(0) is active low) bit is asserted. This forces National's DP83902A to enter the reset state.

5.0 Functional Description (Continued)

5.3 LOGIC DESCRIPTIONS

5.3.1 I/O Card Interface Logic for PCMCIA Host I/O Accesses

This block of logic generates card-side bus control and the appropriate chip-select signals based on the inputs from the PCMCIA host bus. The block's main function is I/O address decoding and operates with the PCMCIA version 2.1 standard. The Function's Base Registers 0,1 and Function Limit Registers 0,1 determine the location and size of the I/O window. Once set up, only PCMCIA accesses to the given function's I/O window will be passed to the device. All control signals are generated for the device for both read and write transactions. The selection of which function receives the PCMCIA transaction is implicit in the PCMCIA address and the particular I/O window the address falls within.

When a function is not selected, CIORD# and CIOWR# are forced to the in-active state. The chip selects CS(0)# and CS(1)# are held in-active for that port also. Once a valid PCMCIA access (read or write) occurs, the control and chip select signals become active.

The condition for an I/O read when a valid address is decoded is:

$$\text{CIORD\#} = \text{HIORD\#} + \text{REG\#} + (\text{CE1\#} * \text{CE2\#})$$

The condition for an I/O write when a valid address is decoded is:

$$\text{CIOWR\#} = \text{HIOWR\#} + \text{REG\#} + (\text{CE1\#} * \text{CE2\#})$$

A DP83903 device with a Revision Code of 001b, in LAN Mode, will decode CS(0) under the same conditions described above for an I/O read as CIORD and for an I/O write as CIOWR#.

5.3.2 EEPROM INTERFACE

*NOTE: The DP83903 operates in both read and write modes with the 16k bit EEPROM only. The DP83903 reads, but cannot write the 4k bit EEPROM. This is due to a subtle difference in the WRITE operation for the two devices. Therefore, it is recommended that the 16k bit EEPROM (NM93C86) be used for card designs which will program the EEPROM after assembly, using the DP83903, and the 4k bit EEPROM (NM93C66) be used **only** on cards which will have the EEPROM written prior to assembly. If an EEPROM write sequence is initiated on a card using the 4k bit EEPROM, the Rdy/Bsy pin on the PCMCIA socket will be held low indefinitely.*

The DP83903 Attribute memory is stored in an external serial CMOS EEPROM that uses the MICROWIRE protocol. Connection to the EEPROM is accomplished using a standard serial EEPROM interface. The DP83903 is compatible with both 8- and 16-bit EEPROM data organizations through use of the EEORG pin. When EEORG is set, the DP83903 is configured for EEPROMs with a 16-bit organization. When EEORG is clear, the DP83903 is configured for EEPROMs with an 8-bit organization. Data transfer is synchronized using the EESK signal whose frequency is equal to $\text{MCLK}(0)/32$. (This allows $f_{\text{EESK}} = 937.5 \text{ kHz}$ using $f_{\text{MCLK}(0)}$ of 30 MHz. Most industry standard EEPROMs specify a maximum clock frequency of 1 MHz.) Data on EEDO and EEDI are latched on the rising edge of EESK. EESK is only generated when the EEPROM is accessed, otherwise it is low.

Read access to the EEPROM is accomplished after a reset or power-up sequence. The DP83903 will not allow any

accesses to the attribute memory (by asserting IREQ# to act as a PCMCIA busy signal) until the EEPROM has been read and placed in the shadow RAM attribute space on the DP83903 IC. Once the read sequences are completed, IREQ# will be de-asserted and the host will be allowed to access the attribute memory space.

Note: Until the DP83903 is configured, which requires the EEPROM be read, it is a memory only interface. During this time, IREQ# is defined as RDY/BSY#.

EEPROM write access is gained by setting the Write EEPROM bit and the Enable EEPROM bit previously set in the EEPROM Control Register. If neither function 0 or function 1 are configured, the DP83903 will then write the contents of the Shadow RAM into the EEPROM. Older data in the EEPROM is lost. During the write back, no accesses to attribute memory are allowed. The EEPROM write back cycle consists of three sequential operations: write enable, write, disable. The DP83903 will not initiate a write back from the Shadow RAM to the EEPROM during a power down condition. Any modification to the CIS (Card Information Structure) to be saved requires the system to initiate a write back.

All EEPROM read/write operations follow a similar sequence: a start bit, some op code, address and data bits. Prior to any operation, EECS is set high. If the RESET signal is pulsed, EEPROM writes are immediately disabled.

To disable access to the EEPROM, there is an Enable EEPROM bit in the EEPROM Control Register. If clear, all EEPROM write accesses will be disabled. The enable bit is disabled as default.

5.3.2.1 CIS Data Security

As a measure to reduce likelihood of accidental EEPROM overwrite the DP83903 EEPROM controller circuit includes a feature which will minimize the jeopardy of corrupting non-volatile CIS data on a card. The Miscellaneous Register located at offset 0x3F0 contains five bits (D4-D0) which are described as the EEPROM State Address. They form the upper five bits of the EEPROM address at which the EEPROM controller circuit will begin writing. These five bits essentially form a "page select." The size of the page depends on the EEPROM size selected. The start address is the byte location in the attribute space (on even boundaries). In order to allow the DP83903 registers to be stored in the EEPROM for auto-configuration of the card at boot-up, the start address must be below the lowest DP83903 Specific Register (Pin Polarity Register at offset 0x3E4), but must also be as high as possible, to protect a maximum amount of CIS data. All data below this start address is write-protected.

In the case of the 2 kB EEPROM, an 11-bit address is required. With the five upper bits programmable (via the Miscellaneous Register), a start address may be formed on 64-bit boundaries anywhere in the 2 kByte space. Starting at address 0x3E4, the next lower 64-bit boundary is at 0x380 (attribute memory space is on even-byte boundaries). To achieve this, the value 0x07 must be programmed into the five LSBs of the Miscellaneous Register. This leaves the lower 448 bytes in the EEPROM protected from overwrite. In the case of an Ethernet LAN card, the Ethernet node ID (6 bytes) should be located in the lower 448 bytes of the attribute memory space, between the CISTPL_END byte and location 0x380. In the case of the 512 Byte EEPROM, a 9-bit address is required. A start address may be formed on

5.0 Functional Description (Continued)

16-bit boundaries anywhere in the 512 Byte space. Starting at address 0x3E4, the next lower 16-bit boundary is at 0x3E0. To achieve this, the value 0x1F must be programmed into the five LSBs of the Miscellaneous Register. This leaves the lower 496 bytes in the EEPROM protected from overwrite.

The method for initializing the EEPROM using the DP83903 is to write the CIS and other protected data (e.g. Ethernet node ID) to the DP83903 attribute memory SRAM and the DP83903 Specific Registers (at offsets 0x3E4 through 0x3F6) from the host system, and the kick off an EEPROM write sequence by writing the value 0x81 to the EEPROM Control Register at offset 0x1002. In order to write the entire EEPROM (starting at address 0), the EEPROM Start Address field in the Miscellaneous Register must be 0x00. This is the value which will be stored in the EEPROM. To implement permanent write protection, a 2nd EEPROM write must be executed after the Start Address field is modified to its final value.

A secondary security feature of the DP83903 is the blocking of EEPROM writes when either function is configured. If the ConfFunc bit (D0) of either Configuration Option Register (located at offset 0x1020 for function 0 and offset 0x1040 for function 1) is set (high), then the DP83903 will not overwrite the EEPROM.

5.3.3 Power Management

The DP83903 supports a hardware power management strategy. This allows the device to switch power on and off based on the activity of each individual function. Each function has a time-out counter set using the CTERM 0,1 Registers. If there has been no PCMCIA Host activity to the given functions I/O window, the function has not requested the card-side bus long enough for that function's timer to expire and no ring or packet indicate occurs, the function will be powered down. This is done by de-asserting the PCNTL() bit (based on its programmed polarity) in the PMGR and Clock Register. Any activity from the function will cause the DP83903 to assert these bits to provide full power to the function and start the clocks. If this activity was a host transaction, the DP83903 will assert HWAIT# for the target function until the DP83903 asserts the PCNTL() signal to power on the function and for 8 FCLK()'s. This gives the function 8 FCLK()s to either power on and respond or at least begin asserting its CWAIT() line. Wake-up activity could be defined as a PCMCIA transaction to the device, a BREQ() from the device, a RI_IN()# if enabled, or a CINT() if enabled. In LAN Mode, a RI_IN(0)# is designated as a packet indicate and is used to check activity.

5.3.4 Bus Arbitration

National's DP83903 IC supports a bus arbitration unit that may arbitrate three possible masters. They are: the PCMCIA Host, Function 0, or Function 1. There are 4 external pins and 2 internal pins for enforcing arbitration decisions. These are BREQ(1:0), BACK(1:0), HBREQ, and HBACK. As described in the registers section, a priority arbitration policy is used.

Each of the three masters may be programmed with a priority from the set (0,1,2,3) independently of the other masters priority. A value of 3 is the highest priority; the value 0 is the lowest. In addition to this, there is also a programmable 8-bit latency timer to guarantee a certain bus ownership time in clocks. If the value is 0, the DP83903 arbiter will follow the

priority policy strictly. Here, a higher priority unit may preempt a lower priority unit by removing its BACK#. A lower priority and equivalent priority unit may not be granted the card-side local bus until the higher priority unit is complete. When the latency timer has a finite value (i.e., 32), a higher priority unit may not be pre-empted from the bus by lower priority units. The difference is that a unit may be pre-empted by higher or equivalent priority units, but, not until the latency timer expires. This guarantees the unit a certain bus time and improves efficiency in high bus traffic systems. The latency timer does not begin counting down until another unit vies for the bus.

If a round-robin arbitration policy is desired, all three units may be set to the same priority with a finite value in the latency timer. Here, any unit may be granted the bus and control it until another unit requires the bus. At that time, the first unit has it until the latency expires and it is removed from the bus (BACK()# de-asserted). The second unit is granted the bus by having its BACK()# asserted.

Note: The destination of a PCMCIA host access (either to function 0 or 1) is implicit in the address and which I/O window it falls within. This steering does not require arbitration, however, it requires that the PCMCIA host is granted access to the card local bus.

5.3.5 Common Memory Management

National's DP83903 has features built in for using a shared common memory architecture on the card. This is useful for functions such as an Ethernet LAN, especially those using a shared memory address space for the packet data area, in which the card's local RAM is mapped into the system memory address space. Using this feature, access to common memory may be granted to either the PCMCIA host or to one of the external functions.

For the PCMCIA host to access the common memory, all that is required is for a PCMCIA Common Memory transaction and bus ownership granted by the DP83903 Arbiter. The DP83903 will perform the PCMCIA requested access. There is no decoding internal to the device to set up Common Memory Windows. Simple decoding can be done external to the DP83903 using address lines. For proper data steering and memory read/write strobing, the DP83903 will check the state of the MemIs8 bit in the Pin Polarity Register to determine the organization of common memory.

If a function desires to access common memory, it requires that it first arbitrate and win the card-side bus. If the LAN Mode bit is clear in Function Configuration Option Register 0, the DP83903 will TRI-STATE MEMWEH# and MEMWEL# any time function 0 or function 1 is granted the bus. When the LAN Mode bit is set, the IC will TRI-STATE MEMWEH# and MEMWEL# when function 1 is granted the bus. The DP83903 will drive MEMWEH# and MEMWEL# when function 0 is granted the bus. In this case MEMWEH# and/or MEMWEL# will be strobed based on MEMWR# being strobed by the LAN. The MemIs8 bit in the Pin Polarity Register will be checked to determine strobing. In all cases, any time a function is granted the bus, the DP83903 will TRI-STATE the MEMOE# signal to allow the bus mastering function to read from the memory. For this scheme to work, each function must TRI-STATE its respective memory write strobe when it is not granted the bus and must connect its read strobe to the MEMOE# signal. Pull-up resistors on the DP83903's MEMOE# output and MEMWR# input will maintain a high level to prevent glitching during bus arbitration.

5.0 Functional Description (Continued)

While the DP83903 will pass any Common Memory access to the 64 Mbyte of common memory space, common memory may be fractured into two ranges, if desired. It will use one address line to select either the shared SRAM described above or another common memory device.

6.0 Operational Modes

6.1 INITIAL SETUP (RESET) AND CONFIGURATION

In order to set up the I/O windows, the Function Base Registers 0, 1 and the Function Limit Registers 0, 1 must be loaded. These registers are loaded with base address information gained from reading the TPCE_IO field within the Card Configuration Table Entry Tuple (CISTPL_CFTABLE_ENTRY, 1Bh) in the CIS (Card Information Structure). This will allow the system software to configure the windows and set the I/O addresses for each function. The software locates the Configuration Option Registers based on address offset values stored in the TPCC_RADR field within the Configuration Tuple (CISTPL_CONFIG, 1Ah) in the CIS. Upon a subsequent read/write operation from the PCMCIA host to the current I/O window address, the DP83903 decodes for a match and then passes the appropriate data, address, and control signals to the appropriate function port. Note, the Attribute memory CIS is initially loaded from the EEPROM upon reset.

6.2 RESET CONDITIONS

When the device is reset using the reset pin, the following actions take place: First, the attribute memory CIS is reloaded from the EEPROM; The Function Configuration Option Registers 0, 1 are reset to a value of 00 Hex; All other registers are set to their default values.

6.3 INTERRUPT CONTROL

For multi-function operation, the DP83903 implements a shared interrupt scheme. The DP83903 will assert PCMCIA IREQ# when either CINT(0) or CINT(1) is asserted. If the Function Configuration Option Register is configured for pulsed mode interrupts, the IREQ# pin will send out a pulse width of period $16/f_{MCLK(0)}$. During multi-function operation, however, level mode interrupts are strongly recommended. The Function Configuration Status Registers indicate which function initiated the interrupt and interrupts will continue until the interrupt requests are processed. This mode would be used if both functions are running at the same time (concurrently).

See the description of the IntrReset bit in the Function Configuration Status Registers 0, 1 for a multi-function interrupt protocol that insures multiple interrupts sharing one IREQ# line are not missed.

6.4 FUNCTIONAL CONCURRENCY

A Dual Function Card may be designed using the DP83903 IC that allows both functions to run concurrently. The

DP83903 bus arbitration unit, interrupt unit, and common memory unit allow functions to take control of the local data bus on the card at their discretion. The bus arbiter will arbitrate between the PCMCIA Host, Function 0, and Function 1. Once granted the bus, each function may gain access to the common memory address space. One technique is to tie each function's Memory Write signal to the DP83903 MEMWR# input. Each function should TRI-STATE its Memory Write if not granted the bus. The DP83903 then generates MEMWEH# and MEMWEL# for memory access. Also, each function may tie its Memory Read to the Common Memory devices (tied to DP83903 MEMOE#). Again, each device should TRI-STATE its Memory Read signal when it is not granted the bus. The DP83903 will TRI-STATE its MEMOE# when the PCMCIA Host has not been granted the bus. Note that both MEMWR# and MEMOE# have pull-up resistors on the DP83903 to prevent glitching.

As mentioned before, once the PCMCIA Host has been granted access to the card bus, the steering of transactions to function 0 or function 1 is implicit in the Address and the I/O Window decoder settings for the DP83903. If Function 0 or 1 has been granted the Card local bus and a PCMCIA host attempts an I/O transaction (i.e. - Host is denied bus), the DP83903 will assert the HWAIT# signal to extend the cycle, de-assert the INPACK# signal, and set the Rdy/Bsy bit in the Pin Replacement Registers.

6.5 16-BIT/8-BIT OPERATION

During normal operation, the DP83903 will function as a 16-bit device. If a LAN IC is used, the LAN should always be configured as a 16-bit device. If 8-bit operation is desired (PCMCIA Host accesses are 8-bit), the DP83903 will pass the 8-bit transaction to the Function. In the case of a 16-bit LAN device, the DP83903 will pass the 8-bit transaction since the LAN IC register access is 8 bits. With the common memory device, the DP83903 will check the Memls8 bit in the Pin Polarity Register. If Memls8 is clear (16-bit memory), the DP83903 will strobe MEMWEL# for 8-bit accesses on even address boundaries and MEMWEH# for 8-bit accesses on odd address boundaries. A 16-bit access causes both MEMWEL# and MEMWEH# to be strobed. A 16-bit LAN device will still execute 16-bit accesses to the Common memory even though PCMCIA is using 8-bit accesses. Due to this, a MEMWR# will cause both MEMWEH# and MEMWEL# to be strobed. This allows the LAN to use 16-bit local DMA with Common Memory. If Memls8 is set (8-bit memory), the DP83903 will strobe MEMWEL# for 8-bit PCMCIA accesses on odd or even address boundaries. For 16-bit access, the DP83903 will only obtain one byte of data by strobing MEMWEL#.

6.6 SPECIAL TESTABILITY MODES

National proprietary. TEST(2:0) pins should be left disconnected.

6.0 Operational Modes (Continued)

Software

System or device software can interact with the DP83903 IC directly using either the DP83903's PCMCIA registers, PCMCIA Extended registers, or DP83903 specific registers.

CIS (CARD INFORMATION STRUCTURE)

When the DP83903 powers on, the contents of the EEPROM are loaded into the device's shadow RAM. This not only allows attribute memory accesses to the CIS, but, it also provides defaults for 10 DP83903 specific registers to be loaded. This allows default loading of parameters that are transparent to system or device software. The best use is for the card manufacturer to determine what values these should be and program them into the EEPROM when the CIS is programmed. Either system software such as Card Services/Socket Services or device software may read and parse the CIS by accessing attribute memory on the PC Card. If desired, this software agent may write to the CIS or default EEPROM registers and, if desired, have these new values saved to the EEPROM. The actual contents of the CIS and the static registers is PC Card design dependent.

PCMCIA REGISTERS

There are two sets of standard PCMCIA Registers which includes the optional I/O Event Register. This allows each function's client software to be able to configure, control, and get status for its respective function. For a detailed description, see the register specifications in this document.

PCMCIA EXTENDED REGISTERS

Each function has a set of base and limit registers. The value placed in these registers by system software controls the I/O Addressing window for each function.

DP83903 SPECIFIC REGISTERS

There are three categories of DP83903 specific registers. The first set of registers are those specific registers that are automatically loaded from the EEPROM and should be transparent to system software. Even though software could be written to modify these registers, the most likely scenario would be the case where software performed macro time scale power management using the PMGR and Clock Register for software power management. The second set are those registers not stored in the EEPROM (such as the ID Register and EEPROM Control Register). These may be accessed by system software as desired using the

attribute memory space. The third set are only accessible when in LAN Mode. This includes the Miscellaneous and Reset Register for use with the LAN Adapter. These registers are mapped to the I/O Memory space within the I/O address window for function 0. These registers should be accessed by a LAN client device driver for the appropriate LAN device and Network Operating System.

INTERRUPT PROTOCOL

The interrupt protocol is defined in the Function Configuration Status Register descriptions. When operating in a multi-function environment, the DP83903 may be placed in an interrupt mode where IREQ# is an "or" of the two CINT()s or where the enhanced interrupt protocol is used. The selection of either mode is done using the IntrReset bit in the Function Configuration Status Registers. For multi-function operation, it's recommended that system software place the DP83903 in the enhanced mode (IntrReset bits set to one (1)). This insures that interrupts can be generated by either function and that they will not be missed by the standard PC-compatible interrupt controller. Of course, either pulse or level mode interrupts may be selected. Once an interrupt occurs, the first system software to be called is the interrupt handler. How this software determines which function generated the interrupt is outside the scope of an IC datasheet, however, mechanisms do exist. For example, software may be written to read the FCSRs to determine the function. Software could also be written to make no determination if it is not required for the particular functions. Finally, software could be written that works in conjunction with the function-specific device interrupt handlers to determine which function requires service without explicitly reading the FCSRs on the DP83903. In either case, system software is responsible for writing a zero (0) to one of the DP83903's Intr bits in an FCSR once interrupt processing is done if the DP83903 is using enhanced interrupts (IntrReset is set to one (1)). This informs the DP83903 that it may generate another interrupt, if one is pending, that will be recognized by the PC-compatible interrupt controller in either pulse or level mode.

BACKWARD COMPATIBILITY

The DP83903 may be operated as a single function PCMCIA interface by using Function 0 only. In this case, the CIS or system software should be written to only configure Function 0.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to 7.0V
DC Input Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	
$V_O = -0.5V$	-0.5V to $V_{CC} + 0.5V$
$V_O = V_{CC} + 0.5V$	
DC Output Source or Sink Current (I_O)	± 12 mA
DC V_{CC} or GND Current /output pin (I_{CC} or I_{GND})	± 6 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J)	140°C

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside these specifications.

Recommended Operating Conditions

Supply Voltage (5.0V V_{CC})	4.75V to 5.25V
Supply Voltage (3.3V V_{CC})	3.00V to 3.60V
DC Input Voltage (V_I)	0.0V to V_{CC}
DC Output Voltage (V_O)	0.0V to V_{CC}
Operating Temperature (T_A)	0°C to +70°C
Minimum Input Edge Rate (dv/dt)	125 mV/ns

Reliability Requirements

Parameter	Conditions	Specification
Electro-Static Discharge	MIL-STD 883	2000V minimum
Latch-Up	MIL-STD 883	

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		Units	Conditions
			Min	Max		
V_{IH}	Minimum High Input Voltage	5.25V 3.6V	2.4 2.0		V	
V_{IL}	Maximum Low Input Voltage	4.75V 3.0V		0.8 0.8	V	
V_{OH}	Minimum High Output Voltage	4.75V 3.0V	0.9 V_{CC} $V_{CC} - 0.2$		V	$I_{OH} = -150 \mu\text{A}$
		4.75V 3.0V	2.8 2.4		V	$I_{OH} = -6$ mA (6 mA Outputs)
V_{OL}	Maximum Low Output Voltage	4.75V 3.0V	0.1 V_{CC} 0.2		V	$I_{OL} = 700 \mu\text{A}$
		4.75V 3.0V	0.4 0.5		V	$I_{OL} = 6$ mA (6 mA Outputs)
I_{IN}	Maximum Input Leakage Current					
	Std. Input I_{IH} I_{IL}	5.25V		+1.0 -1.0	μA	$V_I = V_{CC}, \text{GND}$
	Input w/100k pullup I_{IH} I_{IL}	5.25V		+1.0 -50	μA	$V_I = V_{CC}, \text{GND}$
	Input w/100k pulldown I_{IH} I_{IL}	5.25V		+50 -1.0	μA	$V_I = V_{CC}, \text{GND}$

DC Electrical Characteristics (Continued)

Symbol	Parameter	V _{CC}	T _A = 0°C to +70°C		Units	Conditions
			Min	Max		
I _{OZ}	Maximum Output Leakage Current					
	Std TRI-STATE outputs I _{OZH/L}	5.25V		± 5.0	μA	V _O = V _{CC} , GND
	TRI-STATE output w/10k pull-up I _{OZH} I _{OZL}	5.25V		+ 5.0 - 500	μA	V _O = V _{CC} , GND
I _{OZT}	Maximum I/O Leakage Current					
	Std. I/O I _{OZHT} I _{OZLT}	5.25V		+ 6.0 - 6.0	μA	V _{IO} = V _{CC} , GND
	I/O w/100k pulldown I _{OZHT} I _{OZLT}	5.25V		+ 50 - 6.0	μA	V _{IO} = V _{CC} , GND
I _{HOLD}	Minimum Hold Current (Only Outputs and I/O's with Bus Latch)	4.75V	75 -75		μA	V _I = 0.8V V _I = 2.4V V _I = 0.8V V _I = 2.0V
		3.0V	32 -32			
I _{SWITCH}	Maximum Hold Current Required for Bus Latch to switch	5.25V		± 600	μA	
		3.6V		± 350		
I _{OLD}	Minimum Dynamic Output Current	5.25V	20		mA	V _{OLD} = 30% V _{CC}
		3.6V	10			
I _{OHD}	Minimum Dynamic Output Current	5.25V	-20		mA	V _{OHD} = 70% V _{CC}
		3.6V	-10			
I _{CC}	Maximum Quiescent Supply Current	5.25V		2.0	mA	V _I = V _{CC} , GND
		3.6V		1.25		

Symbol	Parameter	V _{CC}	T _A = 25°C	Units	Conditions
			Typ		
I _{CC1}	I _{CC} per Input—Std. Input	5.25V	1.0	mA	V _I = V _{CC} - 2.1V V _I = V _{CC} - 0.6V
		3.6V	0.5		
I _{CC2}	I _{CC} per Input w/Bus Latch	5.25V	1.0	mA	V _I = V _{CC} - 2.1V V _I = V _{CC} - 0.6V
		3.6V	0.5		
I _{CCD}	Dynamic Power Supply Current	5.25V	6.5	mA	(Note 1)
		3.6V	4.0		

Note 1: The I_{CCD} (Typ) test conditions are to clock MCLK(1:0) at 30 MHz and continuously exercise HADDR(15:0) with a sequential address pattern (0000 to FFFF) at 4.0 MHz. These conditions represent the typical ISA/PCMCIA activity across the PCMCIA socket and simulate the most frequent operation of the card in a system. Note, the MCLK(1:0) and the HADDR(15:0) inputs are driven at a 50% duty cycle with V_I at V_{CC} and 0.0V. All outputs are unloaded.

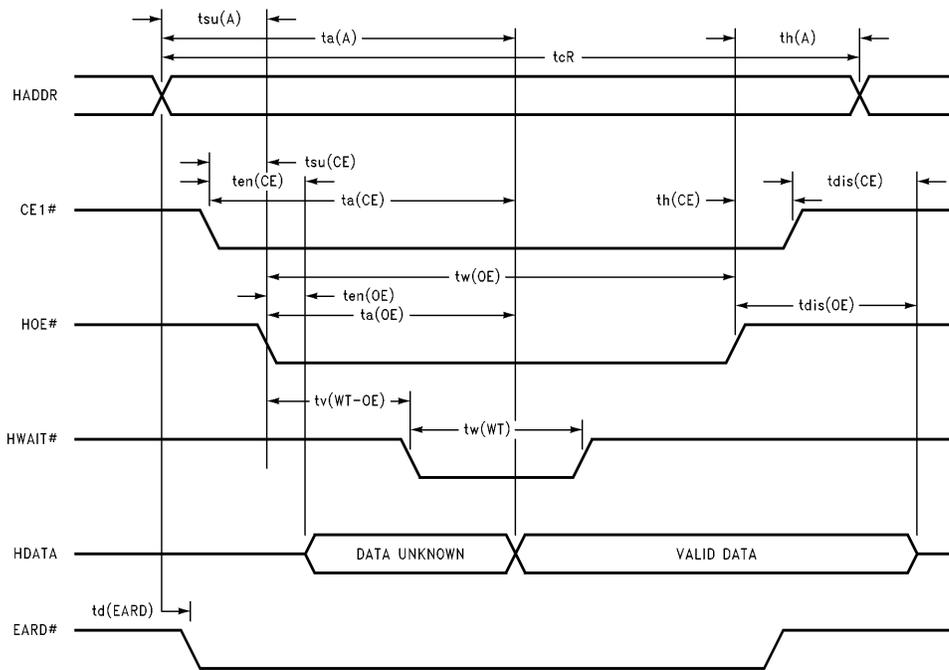


FIGURE 1. Attribute Memory Read Timing

TL/F/12483-5

Attribute Memory Read Timing Specifications (See Figure 1)

Symbol	Path	V _{CC} (V)	Commercial T _A = 0°C to +70°C		Units
			Min	Max	
tcR**	Read Cycle Time	4.75	300		ns
		3.0	300		
ta(A)**	Address Access Time	4.75	300		ns
		3.0	300		
ta(CE)**	CE1 Access Time	4.75	300		ns
		3.0	300		
ta(OE)	Output Enable Access Time	4.75	150		ns
		3.0	150		
tdis(OE)**	Output Disable Time from HOE	4.75	100		ns
		3.0	100		
tdis(CE)	Output Disable Time from CE1	4.75	100		ns
		3.0	100		
ten(OE)**	Output Enable Time from HOE	4.75	5		ns
		3.0	5		
ten(CE)**	Output Enable Time from CE1	4.75	5		ns
		3.0	5		
td(EARD)	EARD Delay from HADDR	4.75	25		ns
		3.0	25		
tsu(A)	Address Setup Time to HOE Falling	4.75	30		ns
		3.0	30		
th(A)**	Address Hold Time from HOE Rising	4.75	20		ns
		3.0	20		
tsu(CE)**	CE1 Setup Time to HOE Falling	4.75	0		ns
		3.0	0		
th(CE)**	CE1 Hold Time from HOE Rising	4.75	20		ns
		3.0	20		
tv(WT-OE)	HWAIT Valid from HOE Falling	4.75	35		ns
		3.0	35		
tw(WT)**	HWAIT Pulse Width	4.75	12000		ns
		3.0	12000		
tw(OE)	HOE Pulse Width	4.75	60		ns
		3.0	70		

**Parameter guaranteed by design.

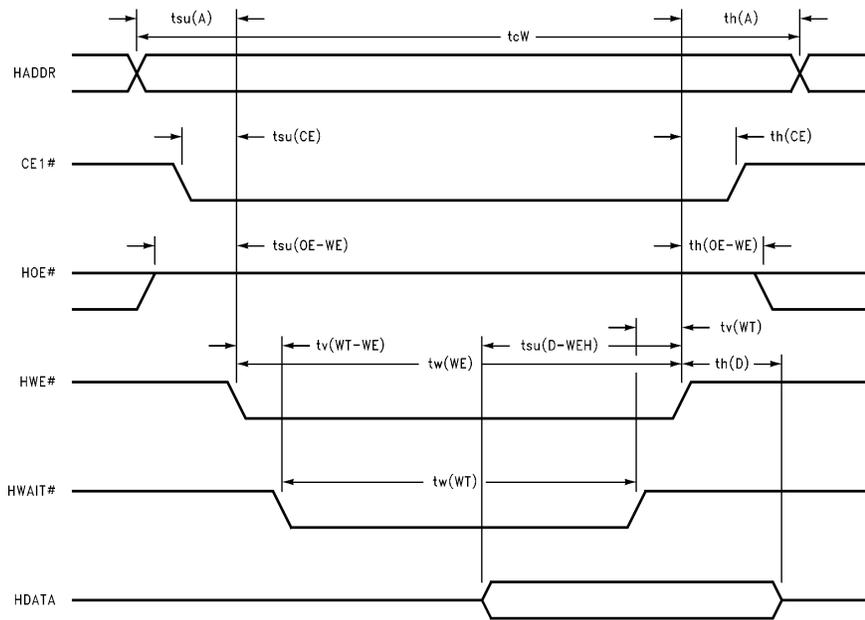


FIGURE 2. Attribute Memory Write Cycle

TL/F/12483-6

Attribute Memory Write Cycle Specifications (See Figure 2)

Symbol	Path	V _{CC} (V)	Commercial T _A = 0°C to +70°C		Units
			Min	Max	
tcW**	Write Cycle Time	4.75	250		ns
		3.0	250		
tw(WE)	Write Enable Pulse Width	4.75	60		ns
		3.0	60		
tsu(A)	HADDR Setup Time to HWE Falling	4.75	30		ns
		3.0	30		
tsu(D-WEH)	HDATA Setup Time to HWE Rising	4.75	10		ns
		3.0	10		
th(D)	HDATA Hold Time from HWE Rising	4.75	15		ns
		3.0	15		
th(A)**	HADDR Hold Time from HWE Rising	4.75	20		ns
		3.0	20		
tsu(OE-WE)**	Output Enable Setup to HWE Falling	4.75	10		ns
		3.0	10		
th(OE-WE)**	Output Enable Hold from HWE Rising	4.75	10		ns
		3.0	10		
tsu(CE)**	CE1 Setup Time to HWE Falling	4.75	0		ns
		3.0	0		
th(CE)**	CE1 Hold Time from HWE Rising	4.75	20		ns
		3.0	20		
tv(WT-WE)	HWAIT Valid from HWE Falling	4.75		35	ns
		3.0		35	
tw(WT)**	HWAIT Pulse Width	4.75		12000	ns
		3.0		12000	
tv(WT)**	HWE High from HWAIT Released	4.75		0	ns
		3.0		0	

**Parameter guaranteed by design.

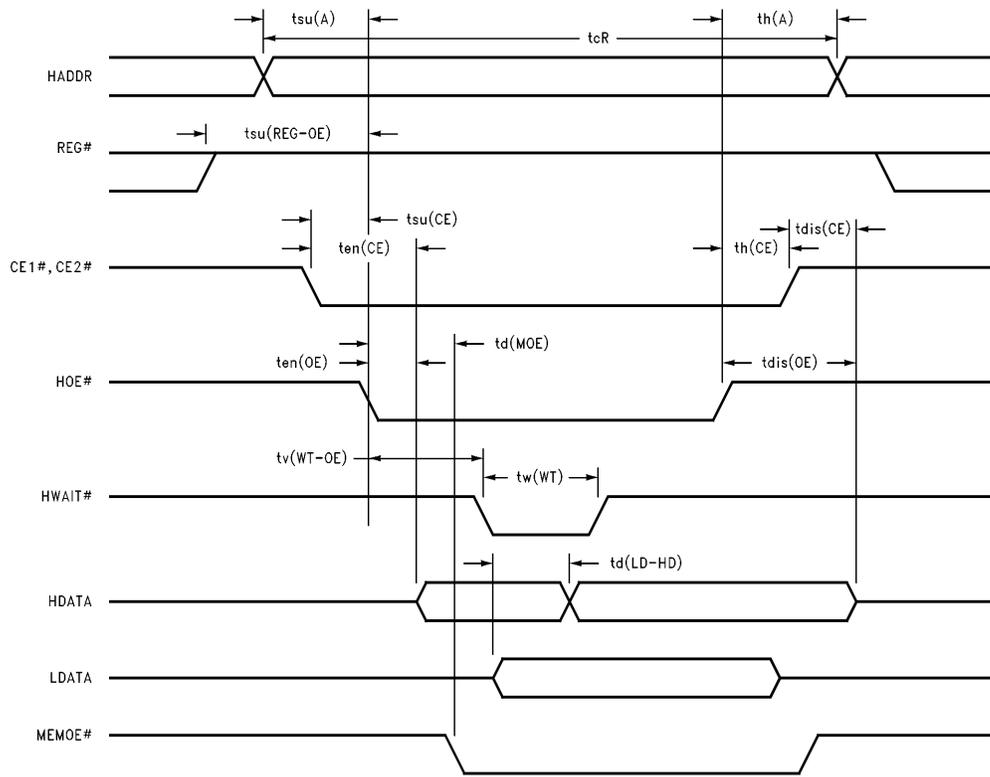


FIGURE 3. Common Memory Read Timing

TL/F/12483-7

Common Memory Read Timing Specifications (See Figure 3)

Symbol	Path	V _{CC} (V)	Commercial T _A = 0°C to +70°C		Units
			Min	Max	
tcR**	Read Cycle Time	4.75	100		ns
		3.0	100		
ten(CE)**	Output Enable from CE Falling	4.75	5		ns
		3.0	5		
ten(OE)**	Output Enable from HOE Falling	4.75	5		ns
		3.0	5		
tsu(A)**	HADDR Setup Time to HOE Falling	4.75	10		ns
		3.0	10		
th(A)**	HADDR Hold Time from HOE Rising	4.75	15		ns
		3.0	15		
tsu(CE)**	CE Setup Time from HOE Falling	4.75	0		ns
		3.0	0		
th(CE)**	CE Hold Time from HOE Rising	4.75	15		ns
		3.0	15		
tv(WT-OE)	HWAIT Valid from HOE Falling	4.75		35	ns
		3.0		35	
tw(WT)**	HWAIT Pulse Width	4.75		12000	ns
		3.0		12000	
tdis(CE)	HDATA Disable from CE Rising	4.75		50	ns
		3.0		50	
tdis(OE)	HDATA Disable from HOE Rising	4.75		50	ns
		3.0		50	
td(MOE)	MEMOE Delay from HOE	4.75		20	ns
		3.0		20	
td(LD-HD)	HDATA Delay from LDATA	4.75		14	ns
		3.0		14	
tsu(REG-OE)**	REG Setup to HOE Falling	4.75	5		ns
		3.0	5		

**Parameter guaranteed by design.

Note: The above Common Memory Read Timing Specifications apply only to 100 ns common memory devices.

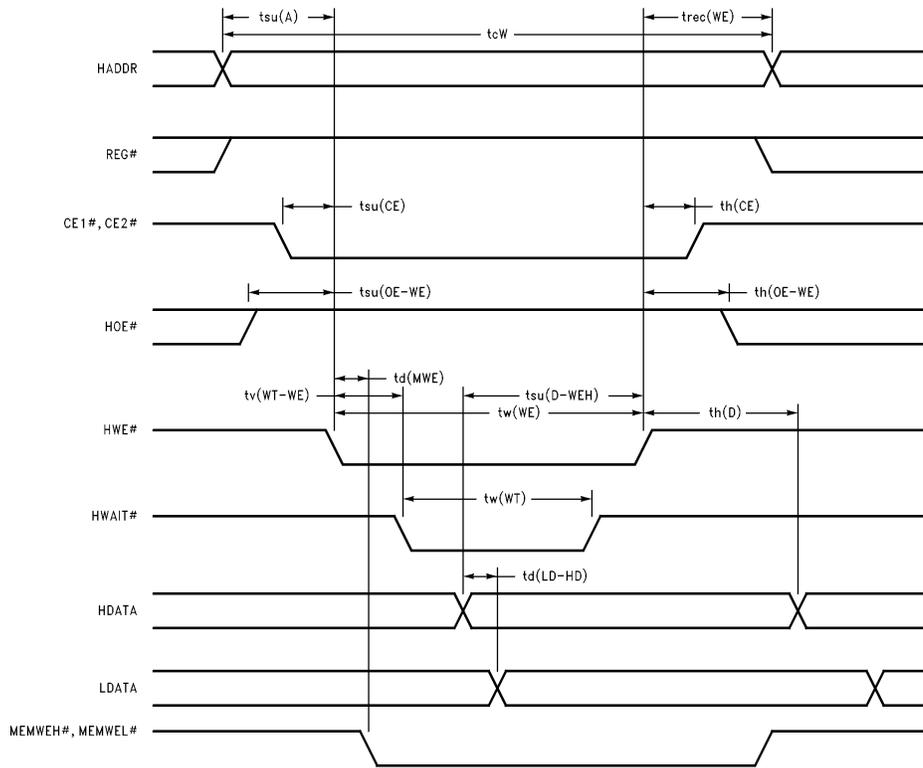


FIGURE 4. Common Memory Write Timing

TL/F/12483-8

Common Memory Write Timing Specifications (See Figure 4)

Symbol	Path	V _{CC} (V)	Commercial T _A = 0°C to +70°C		Units
			Min	Max	
tcW**	Write Cycle Time	4.75	100		ns
		3.0	100		
tw(WE)**	HWE Pulse Width	4.75	60		ns
		3.0	60		
tsu(A)**	HADDR Setup Time from HWE Falling	4.75	10		ns
		3.0	10		
tsu(D-WEH)**	HDATA Setup Time from HWE Rising	4.75	40		ns
		3.0	40		
th(D)**	HDATA Hold Time from HWE Rising	4.75	15		ns
		3.0	15		
trec(WE)**	Write Recovery Time	4.75	15		ns
		3.0	15		
tsu(OE-WE)**	HOE Setup from HWE Falling	4.75	10		ns
		3.0	10		
th(OE-WE)**	HOE Hold from HWE Rising	4.75	10		ns
		3.0	10		
tsu(CE)**	CE Setup Time from HWE Falling	4.75	0		ns
		3.0	0		
th(CE)**	CE Hold Time from HWE Rising	4.75	15		ns
		3.0	15		
tv(WT-WE)	HWAIT Valid from HWE Falling	4.75	35		ns
		3.0	35		
tw(WT)**	HWAIT Pulse Width	4.75	12000		ns
		3.0	12000		
td(MWE)	MEMWEH, MEMWEL Delay from HWE	4.75	20		ns
		3.0	20		
td(LD-HD)	LDATA Delay from HDATA	4.75	15		ns
		3.0	15		

**Parameter guaranteed by design.

Note: The above Common Memory Write Timing Specifications apply only to 100 ns SRAM common memory devices. Common memory devices such as OTPROM, EPROM and Flash do not have standard programming specifications.

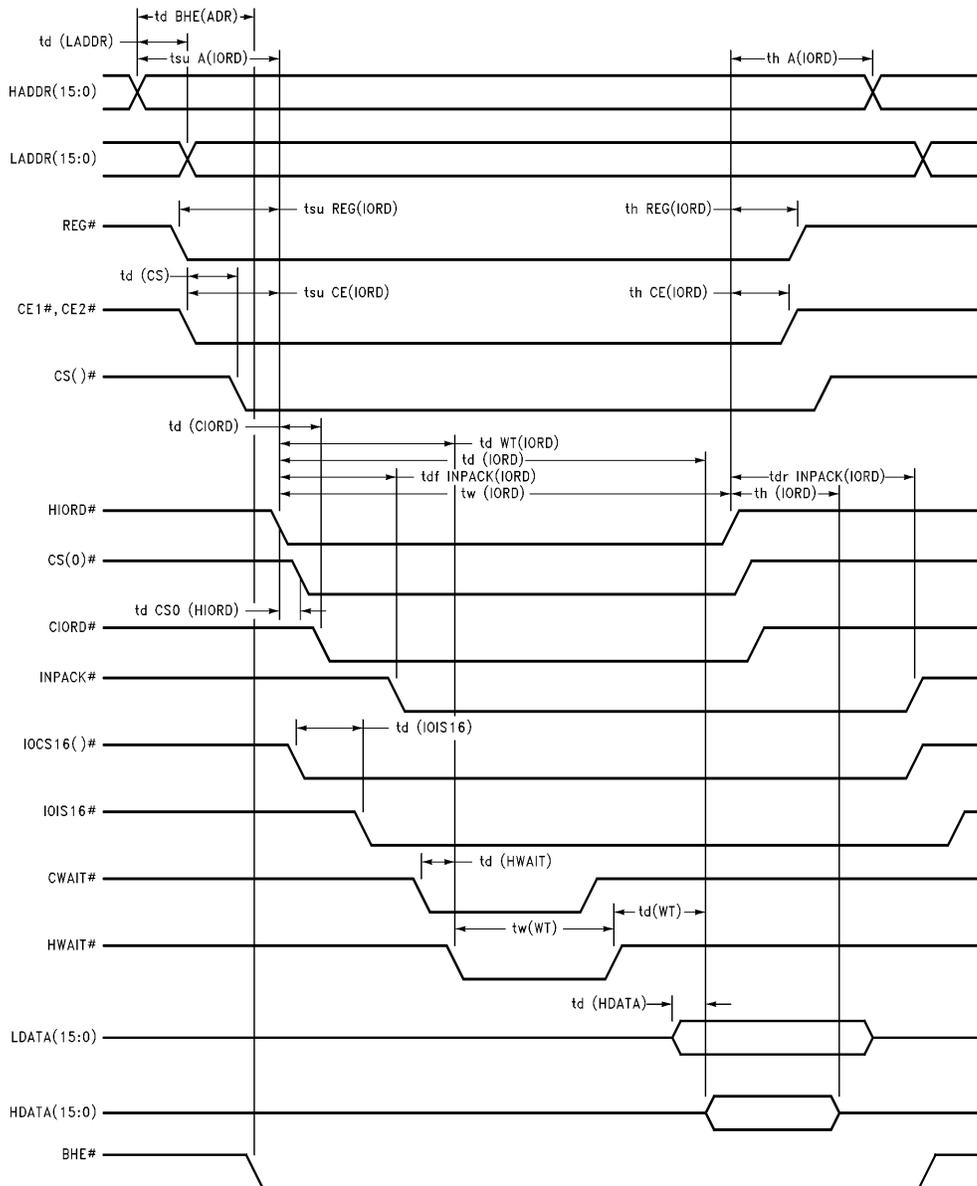


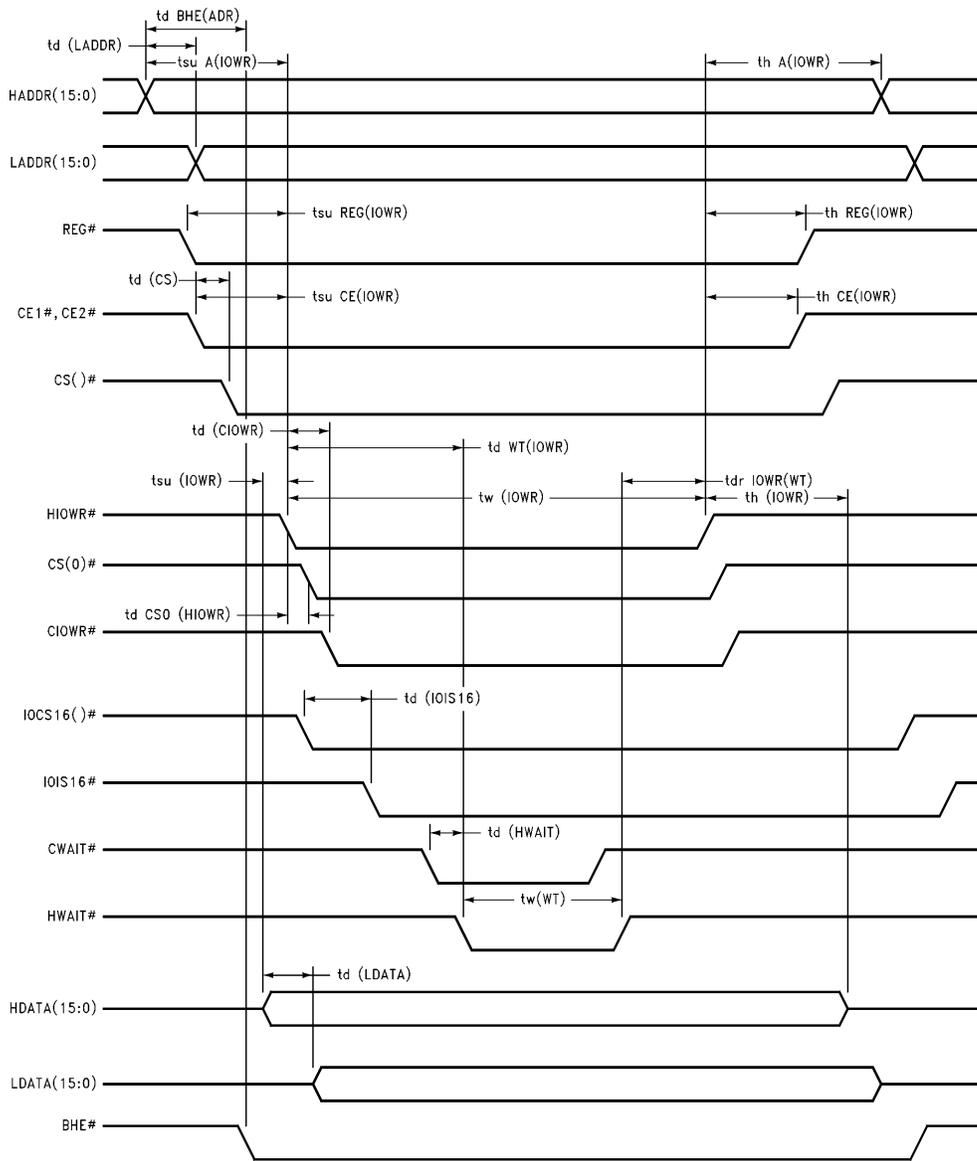
FIGURE 5. I/O Read Timing Specification

TL/F/12483-9

I/O Read Timing Specifications (See Figure 5)

Symbol	Path	V _{CC} (V)	Commercial T _A = 0°C to +70°C		Units
			Min	Max	
tsu REG(IORD)**	REG Setup to HIORD Falling	4.75	5		ns
		3.0	5		
tsu CE(IORD)**	CE Setup to HIORD Falling	4.75	5		ns
		3.0	5		
tsu A(IORD)**	HADDR Setup to HIORD Falling	4.75	70		ns
		3.0	70		
tw (IORD)	HIORD Pulse Width	4.75	165		ns
		3.0	165		
tdf INPACK(IORD)	INPACK Delay from HIORD Falling	4.75	45		ns
		3.0	45		
td(IORD)	HDATA Access from HIORD Falling	4.75	100		ns
		3.0	100		
tw(WT)**	HWAIT Pulse Width	4.75	12000		ns
		3.0	12000		
td WT(IORD)	HWAIT Delay from HIORD Falling	4.75	35		ns
		3.0	35		
td(WT)**	HDATA Delay from WAIT Release	4.75	35		ns
		3.0	35		
th A(IORD)**	HADDR Hold from HIORD Rising	4.75	20		ns
		3.0	20		
th REG(IORD)**	REG Hold from HIORD Rising	4.75	0		ns
		3.0	0		
th CE(IORD)**	CE Hold from HIORD Rising	4.75	20		ns
		3.0	20		
tdr INPACK(IORD)	INPACK Delay from HIORD Rising	4.75	45		ns
		3.0	45		
th(IORD)**	HDATA Hold from HIORD Rising	4.75	0		ns
		3.0	0		
td(CS)	CS Delay from CE Falling	4.75	20		ns
		3.0	30		
td(CIORD)	CIORD Delay from HIORD	4.75	25		ns
		3.0	35		
td CS0 (HIORD)	CS(0) Delay from HIORD # . LAN Mode Only	4.75	15		ns
		3.0	20		
td(HDATA)	HDATA Delay from LDATA	4.75	20		ns
		3.0	25		
td BHE(ADR)	BHE Delay from HADDR	4.75	20		ns
		3.0	25		
td(IOIS16)	IOIS16 Delay from IOCS16 Falling	4.75	13		ns
		3.0	13		
td(HWAIT)	HWAIT Delay from CWAIT	4.75	25		ns
		3.0	30		
td(LADDR)	LADDR Delay from HADDR	4.75	20		ns
		3.0	25		

**Parameter guaranteed by design.



TL/F/12483-10

FIGURE 6. I/O Write Timing Specification

I/O Write Timing Specifications (See Figure 6)

Symbol	Path	V _{CC} (V)	Commercial T _A = 0°C to +70°C		Units
			Min	Max	
tsu REG(IOWR)	REG Setup to HIOWR Falling	4.75	5		ns
		3.0	5		
tsu CE(IOWR)**	CE Setup to HIOWR Falling	4.75	5		ns
		3.0	5		
tsu A(IOWR)	HADDR Setup to HIOWR Falling	4.75	70		ns
		3.0	70		
tsu(IOWR)	HDATA Setup to HIOWR Falling	4.75	60		ns
		3.0	60		
tw(IOWR)	HIOWR Pulse Width	4.75	165		ns
		3.0	165		
tw(WT)**	HWAIT Pulse Width	4.75	12000		ns
		3.0	12000		
td WT(IOWR)	HWAIT Delay from HIOWR Falling	4.75	35		ns
		3.0	35		
th A(IOWR)**	HADDR Hold from HIOWR Rising	4.75	20		ns
		3.0	20		
th REG(IOWR)**	REG Hold from HIOWR Rising	4.75	0		ns
		3.0	0		
th CE(IOWR)**	CE Hold from HIOWR Rising	4.75	20		ns
		3.0	20		
th(IOWR)**	HDATA Hold from HIOWR Rising	4.75	30		ns
		3.0	30		
td(LADDR)	LADDR Delay from HADDR	4.75	20		ns
		3.0	25		
td(CS)	CS Delay from CE Falling	4.75	20		ns
		3.0	25		
td(CIOWR)	CIOWR Delay from HIOWR Falling	4.75	25		ns
		3.0	30		
td CSO (HIOWR)	CS(0) Delay from HIOWR #. LAN Mode Only	4.75	15		ns
		3.0	20		
td(LDATA)	LDATA Delay from HDATA	4.75	20		ns
		3.0	25		
td BHE(ADR)	BHE Delay from HADDR	4.75	20		ns
		3.0	25		
td(IOIS16)	IOIS16 Delay from IOCS16 Falling	4.75	13		ns
		3.0	13		
td(HWAIT)	HWAIT Delay from CWAIT	4.75	25		ns
		3.0	30		
tdr IOWR(WT)**	HIOWR Rise from HWAIT Release	4.75	0		ns
		3.0	0		

**Parameter guaranteed by design.

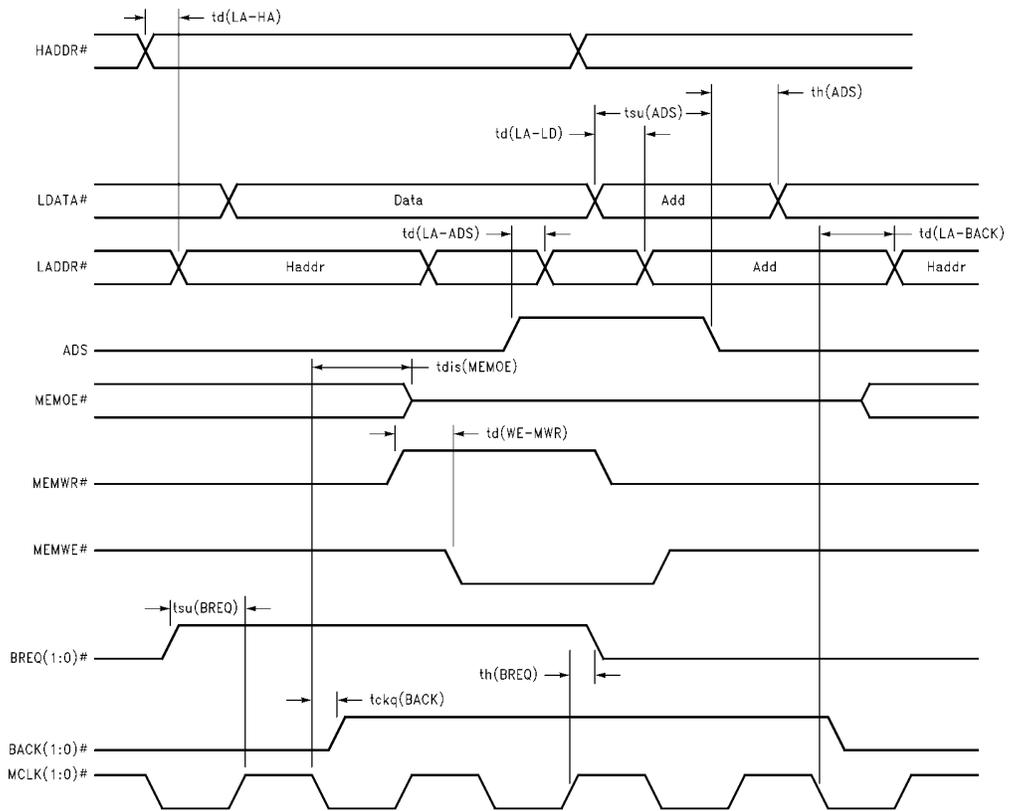


FIGURE 7. Bus Arbitration Timing

TL/F/12483-11

Bus Arbitration Timing Specifications (See Figure 7)					
Symbol	Path	V_{CC} (V)	Commercial T_A = 0°C to +70°C		Units
			Min	Max	
td(LA-ADS)	LADDR Valid from ADS	4.75		20	ns
		3.0		20	
td(LA-HA)	LADDR Delay from HADDR	4.75		15	ns
		3.0		15	
td(LA-LD)	LADDR Delay from LDATA	4.75		18	ns
		3.0		18	
tckq(BACK)	BACK Delay from MCLK Falling	4.75		30	ns
		3.0		35	
td(WE-MWR)	MEMWEH Delay from MEMWR	4.75		17	ns
		3.0		20	
td(WE-MWR)	MEMWEL Delay from MEMWR	4.75		17	ns
		3.0		20	
tdis(MEMOE)	MEMOE Disable Time from MCLK Falling	4.75		195	ns
		3.0		160	
tsu(ADS)	LDATA Setup Time to ADS Falling	4.75	13		ns
		3.0	13		
th(ADS)	LDATA Hold Time to ADS Falling	4.75	10		ns
		3.0	10		
tsu(BREQ)	BREQ Setup Time to MCLK Rising	4.75	13		ns
		3.0	13		
th(BREQ)	BREQ Hold Time to MCLK Rising	4.75	13		ns
		3.0	13		
td(LA-BACK)	LADDR Delay from MCLK Falling	4.75		35	ns
		3.0		45	

DP83903 IC Specific Timing Specifications

Symbol	Path	V _{CC} (V)	Commercial T _A = 0°C to +70°C		Units
			Min	Max	
td(CS)	CS(0)/CS(1) from Valid Address	4.75		30	ns
		3.0		40	
td(IREQ)	IREQ Delay from CINT	4.75		20	ns
		3.0		25	
td(SPKR)	SPKR Delay from SPK_IN	4.75		17	ns
		3.0		20	
td(PORT)	DPORT Delay from HWE	4.75		35	ns
		3.0		40	
td(SRESET)	SRESET(1:0) Delay from RESET	4.75		30	ns
		3.0		35	
td(PCNTL)	PCNTL(0) Delay from HWE	4.75		35	ns
		3.0		40	
td(FCLK)	FCLK(1:0) Delay from MCLK(1:0)	4.75		25	ns
		3.0		30	
Frequency	MCLK(1:0)	4.75	5	30	MHz
		3.0	5	30	
Skew**	FCLK(1:0) when MCLK(1:0) Tied	4.75		5.0	ns
		3.0		5.0	

**Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typical	Units	Conditions
C _{IN}	Input Pin Capacitance	3	pF	V _{CC} = OPEN
C _{OUT}	Output Pin Capacitance	5	pF	V _{CC} = 5.0V
C _{I/O}	Input/Output Capacitance	5	pF	V _{CC} = 5.0V
C _{PD}	Power Dissipation Capacitance	42	pF	V _{CC} = 5.0V

Typical Applications

Dual Function Card with the National DP83902A LAN and Rockwell RC224ATF Modem.

2. RC224ATF Modem Designer's Guide, Rockwell Databook.

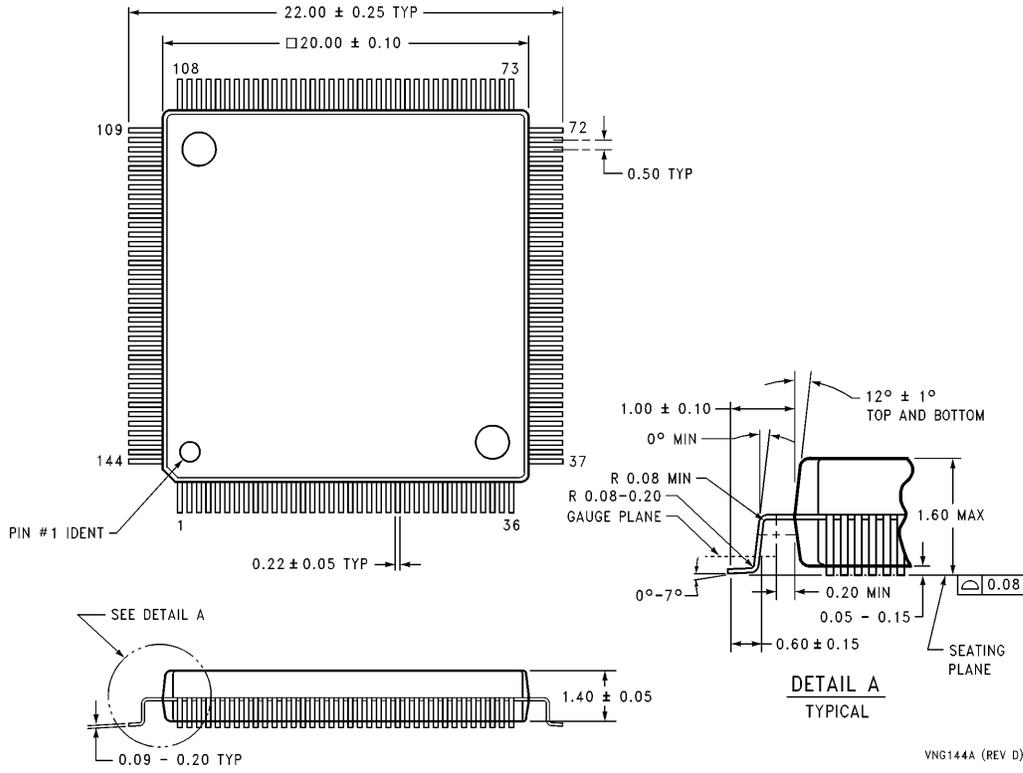
3. PCMCIA PC Card Standard – Release 2.1

4. National Semiconductor 1992 Memory Databook. Application Note AN758.

References

1. National DP83902A Serial Network Interface Controller for Twisted Pair DP83902A Datasheet, 1993 National LAN Databook.

Physical Dimensions millimeters



144-Pin TQFP
144-Lead (20mm x 20mm) Molded Thin Plastic Quad Flat Package, (JEDEC)
NS Package Number VNG144A

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National Semiconductor Corporation
 1111 West Bardin Road
 Arlington, TX 76017
 Tel: 1(800) 272-9959
 Fax: 1(800) 737-7018

National Semiconductor Europe
 Fax: (+49) 0-180-530 85 86
 Email: cnjwge@tevm2.nsc.com
 Deutsch Tel: (+49) 0-180-530 85 85
 English Tel: (+49) 0-180-532 78 32
 Français Tel: (+49) 0-180-532 93 58
 Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
 19th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
 Fax: (852) 2736-9960

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