RL5C475/RT5C475/RC5C475

PCI-CARDBUS BRIDGE

DATA SHEET

REV. 1.1a

RICOH

Designed for Microsoft® Windows NT® Windows® 95

REVISION HISTORY

REVISION	DATE	COMMENTS
1.0	6/2/98	Final specification version 1.0
1.1	6/18/98	TQFP Package support. Reset conditions are defined on Misc Control 1, Subsystem Vendor ID and Subsystem ID registers.
1.1a	8/3/98	The misrepresentation of CE1# and CE2# is corrected.

1 OVERVIEW

The 5C475 is a PC card controller offering a single chip solution as a bridge between PCI bus and CardBus. The 5C475 includes a PC Card 95 compliant socket interface and a bridge function to the PCI bus of 33Mhz. The 5C475 can support the 32-bit CardBus(Card-32) and the 16-bit PC card(Card-16) without external buffers.

Concerning the card control interface, the 5C475's register is compatible with the Intel 82365SL and Ricoh's RF5C396/366 in order to maintain backward compatibility with the existing 16-bit PC Card compliant with PCMCIA2.1/JEIDA4.2. All PC card interface signals are individually buffered to allow direct connection to CardBus and Hot insertion/removal without external buffers. The 5C475 also allows direct connection to PCI bus.

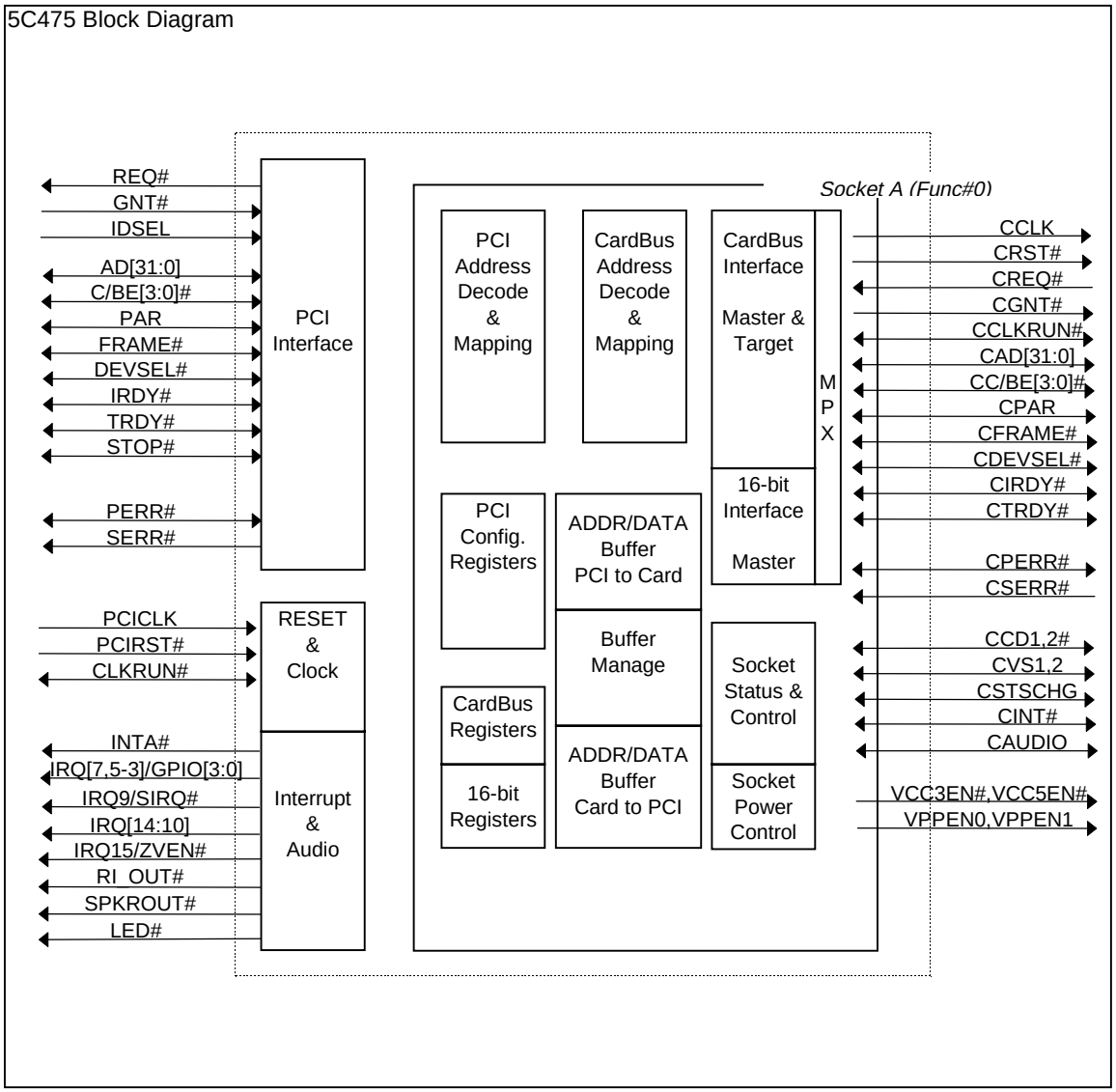
The PCI interface and PC card socket interface have their own power supply terminals that can be powered at either 3.3V or 5V for compatibility with 3.3V and 5V signaling environments. The core logic is powered at 3.3V.

The 5C475 allows the system to be equipped with the high performance multimedia PC cards like the Video capture card.

- PC98 compliant
  - PC98 Design Guide compliant (Subsystem ID, Subsystem Vender ID)
  - ACPI 1.0 and PCI Bus Power Management 1.0 compliant
- Low Power consumption
  - Hardware Suspend
  - CLKRUN#,CCLKRUN# support
- High-performance
- Single Chip PCI-CardBus Bridge
  - PCMCIA PC-Card 95 socket support
  - CardBus(Card-32) Card and 16-bit(PCMCIA2.1/JEIDA4.2) Card support
- PCI Bus Interface
  - Compliant with PCI Local Bus Specification2.1
  - The maximum frequency 33MHz
  - PCI Master/Target protocol support
  - Direct connection to PCI bus
- CardBus PC card Bridge
  - Compliant with PCMCIA PC Card 95/CardBus Standard Specification
  - Compliant with Yenta register set Rev2.2
  - The maximum frequency 33MHz
  - CardBus Master/Target protocol support
  - Transfer transactions
    - All memory read/write transaction(bi-direction)
    - I/O read/write transaction(bi-direction)
    - Configuration read/write transaction(PCI $\rightarrow$ Card)
    - 2 programmable memory windows
    - 2 programmable I/O windows
- PC Card-16 Bridge
  - Compliant with PCMCIA PC Card 95 CardBus(PC Card-16) Standard Specification
  - 5 programmable memory windows
  - 2 programmable I/O windows
  - Compliant with i82365SL compatible register set / ExCA TM
- System Interrupt
  - INTA# support for PCI system interrupt
  - IRQn support for ISA system interrupt (Non shared IRQn pins)
  - Serialized IRQ support

- 3.3V/5V Mixed Voltage Operation at 33Mhz
- GPIO support
- Posting Write and Prefetching Read support
- Plug and Play support
- 16-bit Legacy mode (3E0/3E2 I/O port) support
- PCIway Legacy DMA support
- Package
  - 144pin LQFP 20mm × 20mm 0.5mm pin pitch t=1.7mm
  - 144pin TQFP 16mm × 16mm 0.4mm pin pitch t=1.27mm
  - 144pin CSP 12mm × 12mm 0.8mm pin pitch t=1.2mm

2 BLOCK DIAGRAM



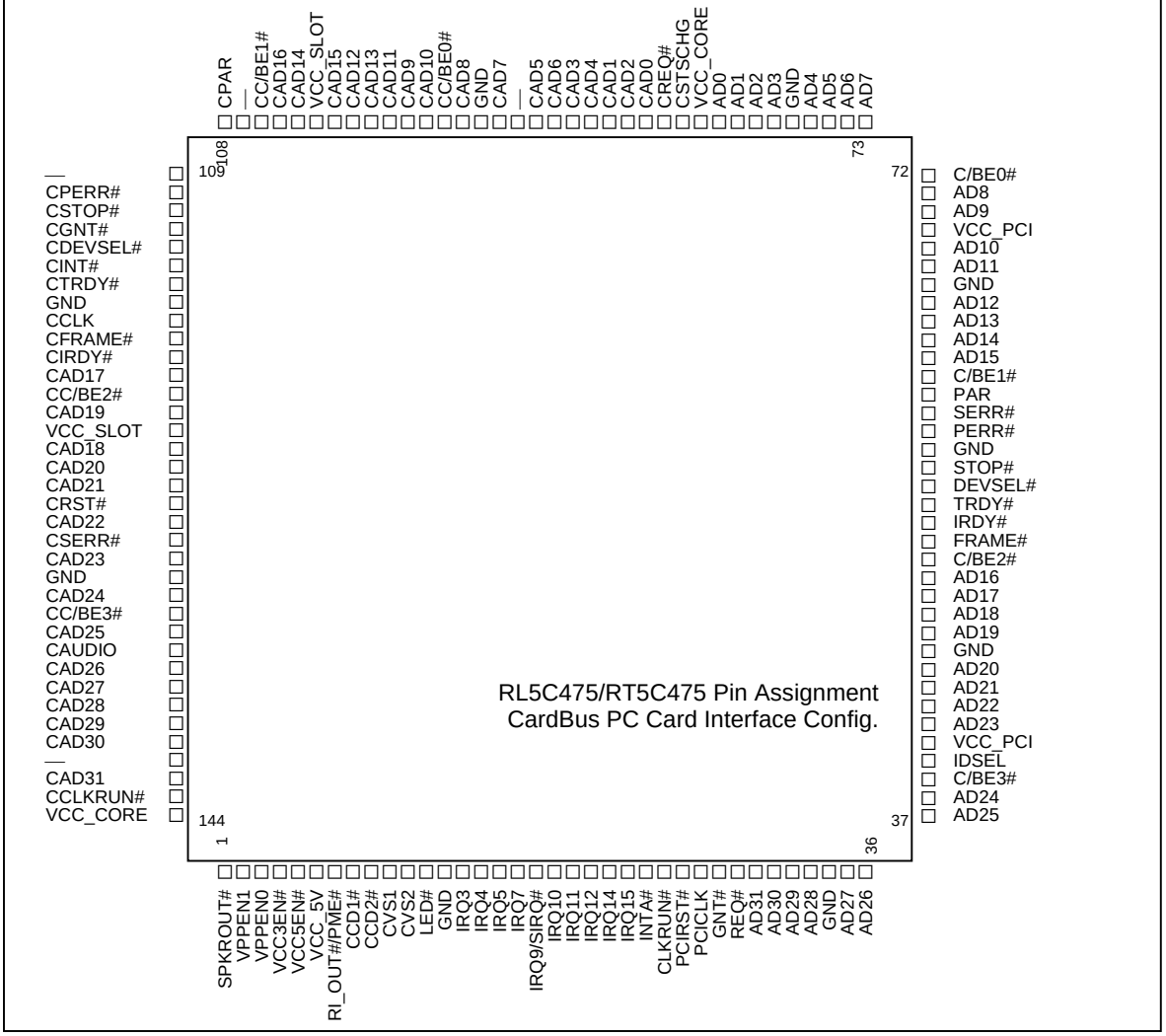
3 PIN DESCRIPTION

3.1 Pin Assignments

3.1.1 RL5C475 / RT5C475 pin assignment

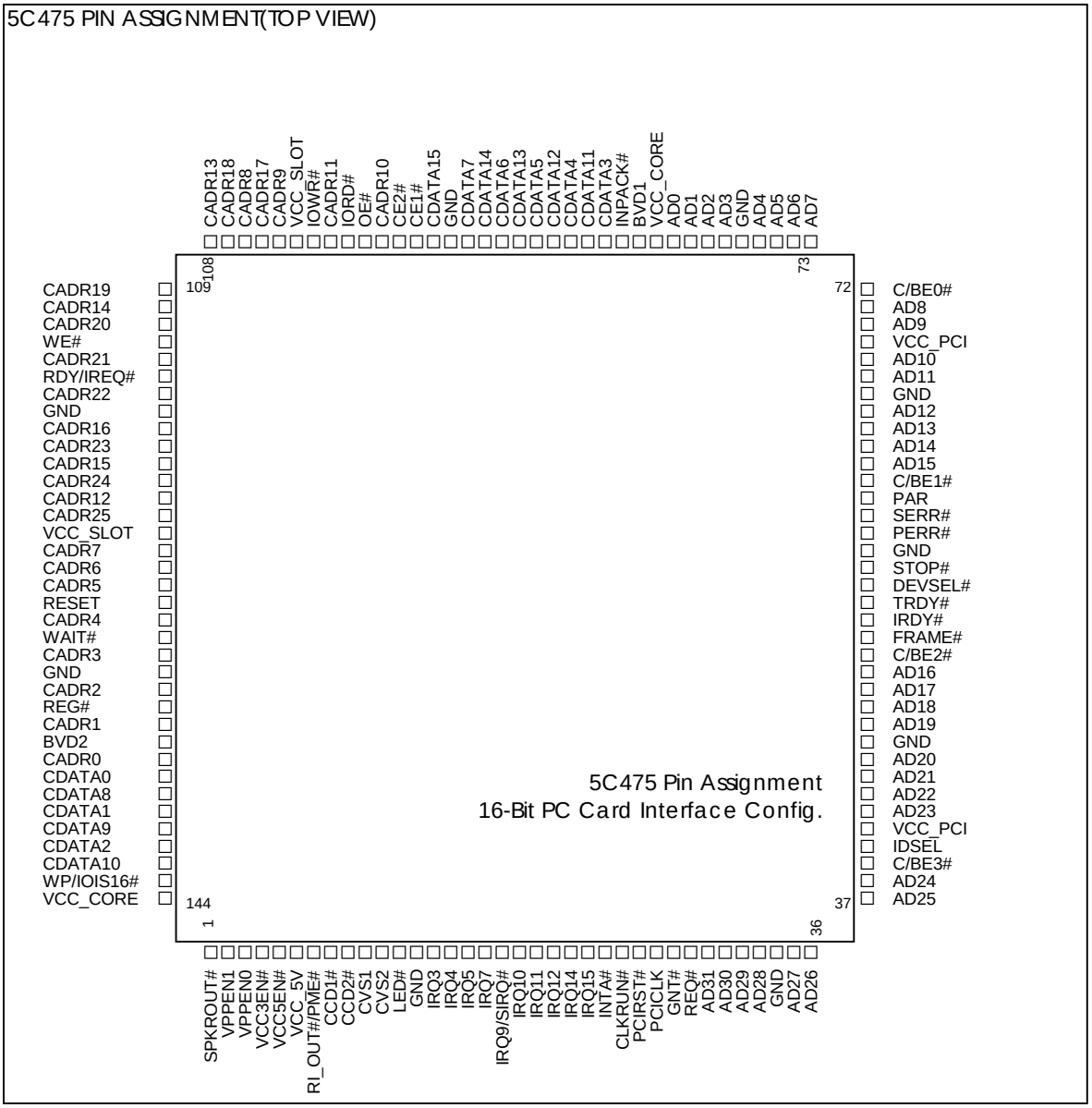
32bit PC Card I/F

RL5C475/RT5C475 PIN ASSIGNMENT(TOP VIEW)



16bit PC Card I/F

5C475 PIN ASSIGNMENT(TOP VIEW)



3.1.2 RC5C475 pin assignment

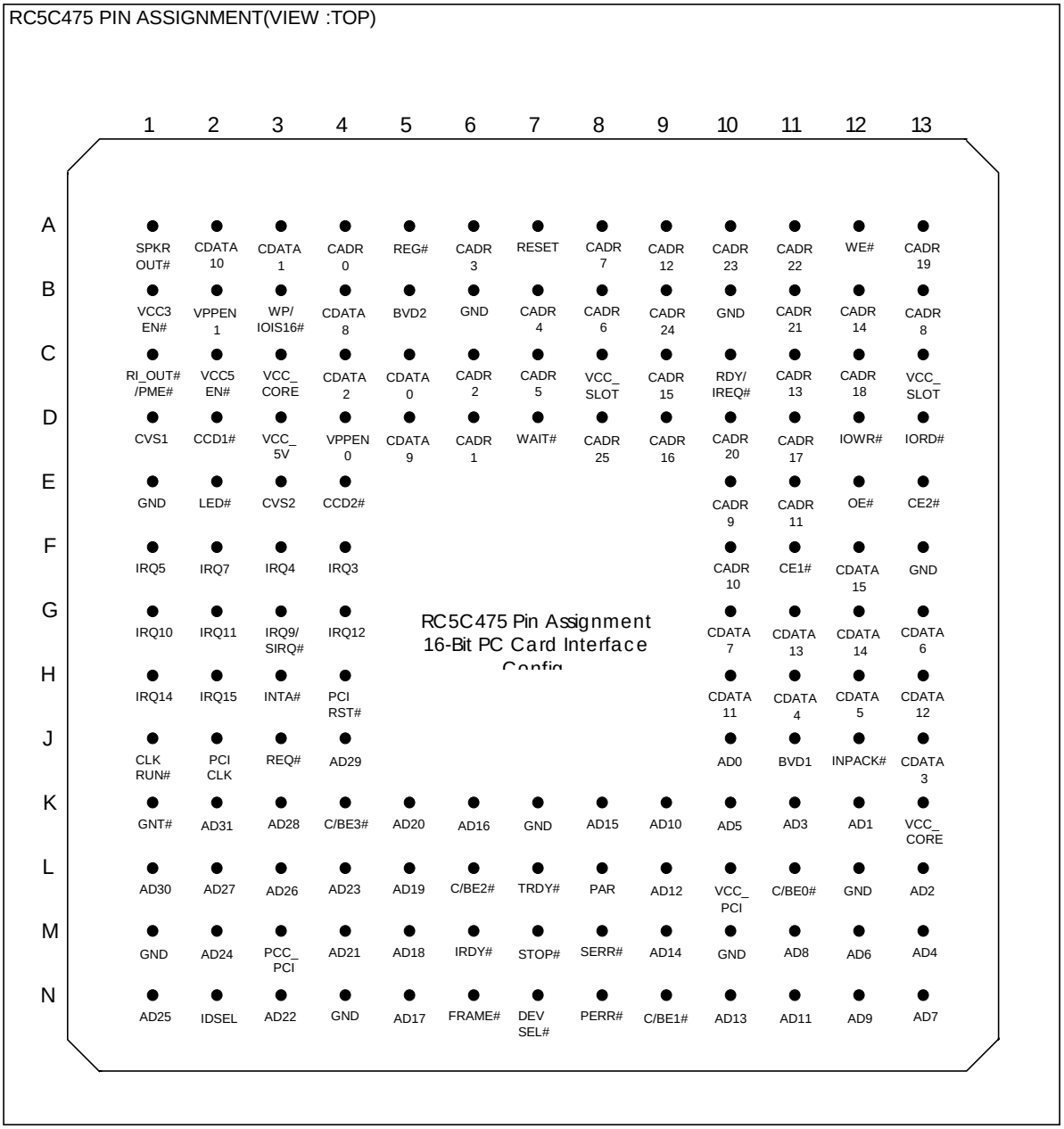
32bit PC Card I/F

RC5C475 PIN ASSIGNMENT(VIEW : TOP)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	SPKR OUT#	CAD31	CAD29	CAD26	CC/ BE3#	CAD23	CRST#	CAD18	CC/ BE2#	CFRA ME#	CTRDY#	CGNT#	-
B	VCC3 EN#	VPPEN 1	CCLK RUN#	CAD28	CAUDIO	GND	CAD22	CAD20	CAD17	GND	CDEV SEL#	CPERR#	CC/ BE1#
C	RI_OUT# /PME#	VCC5 EN#	VCC_ CORE	-	CAD27	CAD24	CAD21	VCC_ SLOT	CIRDY#	CINT#	CPAR	-	VCC_ SLOT
D	CVS1	CCD1#	VCC_ 5V	VPPEN 0	CAD30	CAD25	CSERR#	CAD19	CCLK	CSTOP#	CAD16	CAD15	CAD13
E	GND	LED#	CVS2	CCD2#						CAD14	CAD12	CAD11	CAD10
F	IRQ5	IRQ7	IRQ4	IRQ3						CAD9	CC/ BE0#	CAD8	GND
G	IRQ10	IRQ11	IRQ9/ SIRQ#	IRQ12	RC5C475 Pin Assignment CardBus PC Card Interface Config.					CAD7	CAD6	-	CAD5
H	IRQ14	IRQ15	INTA#	PCI RST#						CAD2	CAD1	CAD3	CAD4
J	CLK RUN#	PCI CLK	REQ#	AD29						AD0	CSTS CHG	CREQ#	CAD0
K	GNT#	AD31	AD28	C/BE3#	AD20	AD16	GND	AD15	AD10	AD5	AD3	AD1	VCC_ CORE
L	AD30	AD27	AD26	AD23	AD19	C/BE2#	TRDY#	PAR	AD12	VCC_ PCI	C/BE0#	GND	AD2
M	GND	AD24	PCC_ PCI	AD21	AD18	IRDY#	STOP#	SERR#	AD14	GND	AD8	AD6	AD4
N	AD25	IDSEL	AD22	GND	AD17	FRAME#	DEV SEL#	PERR#	C/BE1#	AD13	AD11	AD9	AD7

16bit PC Card I/F

RC5C475 PIN ASSIGNMENT(VIEW :TOP)



3.2 5C475 Pin Characteristics

Pin No.	Ball No.	16-bit Card Interface		CardBus Card Interface		Pin Characteristics					Note
		Pin Name	Dir	Pin Name	Dir	Type	Pwr Rail	Pullup 16 / CB	Pulldown 16 / CB	Drive	
1	A1	SPKROUT# HWSUSP#	I/O	SPKROUT# HWSUSP#	I/O	I/O	5			4mA	
2	B2	VPPEN1	O	VPPEN1	O	O	5			4mA	
3	D4	VPPEN0	O	VPPEN0	O	O	5			4mA	
4	B1	VCC3EN#	O	VCC3EN#	O	O	5			4mA	
5	C2	VCC5EN#	O	VCC5EN#	O	O	5			4mA	
6	D3	VCC_5V	DC in	VCC_5V	DC in	PWR	5			—	
7	C1	RI_OUT#/ PME#	O	RI_OUT#/ PME#	O	O(OD)	5			4mA	
8	D2	CCD1#	I	CCD1#	I	I(PU)	5	PU	PU	—	
9	E4	CCD2#	I	CCD2#	I	I(PU)	5	PU	PU	—	
10	D1	CVS1	I/O	CVS1	I/O	I/O	5			1mA	
11	E3	CVS2	I/O	CVS2	I/O	I/O	5			1mA	
12	E2	LED#	O	LED#	O	O	5			8mA	
13	E1	GND	DC in	GND	DC in	PWR	G			—	
14	F4	IRQ3/GPIO0	I/O	IRQ3/GPIO0	I/O	I/O	P			8mA	
15	F3	IRQ4/GPIO1	I/O	IRQ4/GPIO1	I/O	I/O	P			8mA	
16	F1	IRQ5/GPIO2	I/O	IRQ5/GPIO2	I/O	I/O	P			8mA	
17	F2	IRQ7/GPIO3	I/O	IRQ7/GPIO3	I/O	I/O	P			8mA	
18	G3	IRQ9/SIRQ#	I/O	IRQ9/SIRQ#	I/O	I/O	P			8mA	
19	G1	IRQ10	O	IRQ10	O	O(TS)	P			8mA	
20	G2	IRQ11	O	IRQ11	O	O(TS)	P			8mA	
21	G4	IRQ12	O	IRQ12	O	O(TS)	P			8mA	
22	H1	IRQ14	O	IRQ14	O	O(TS)	P			8mA	
23	H2	IRQ15/ ZVEN#	O	IRQ15/ ZVEN#	O	O(TS)	P			8mA	
24	H3	INTA#	O	INTA#	O	O(OD)	P			PCI21	
25	J1	CLKRUN#	I/O	CLKRUN#	I/O	I/O	P			PCI21	
26	H4	PCIRST#	I	PCIRST#	I	I	P			—	
27	J2	PCICLK	I	PCICLK	I	I	P			—	
28	K1	GNT#	I	GNT#	I	I	P			—	
29	J3	REQ#	O	REQ#	O	O(TS)	P			PCI21	
30	K2	AD31	I/O	AD31	I/O	I/O	P			PCI21	
31	L1	AD30	I/O	AD30	I/O	I/O	P			PCI21	
32	J4	AD29	I/O	AD29	I/O	I/O	P			PCI21	
33	K3	AD28	I/O	AD28	I/O	I/O	P			PCI21	
34	M1	GND	DC in	GND	DC in	PWR	G			—	
35	L2	AD27	I/O	AD27	I/O	I/O	P			PCI21	
36	L3	AD26	I/O	AD26	I/O	I/O	P			PCI21	

Pin No.	Ball No.	16-bit Card Interface		CardBus Card Interface		Pin Characteristics					Note
		Pin Name	Dir	Pin Name	Dir	Type	Pwr Rail	Pullup Pulldown 16 / CB		Drive	
37	N1	AD25	I/O	AD25	I/O	I/O	P			PCI21	
38	M2	AD24	I/O	AD24	I/O	I/O	P			PCI21	
39	K4	C/BE3#	I/O	C/BE3#	I/O	I/O	P			PCI21	
40	N2	IDSEL	I	IDSEL	I	I	P			—	
41	M3	VCC_PCI	DC in	VCC_PCI	DC in	PWR	P			—	
42	L4	AD23	I/O	AD23	I/O	I/O	P			PCI21	
43	N3	AD22	I/O	AD22	I/O	I/O	P			PCI21	
44	M4	AD21	I/O	AD21	I/O	I/O	P			PCI21	
45	K5	AD20	I/O	AD20	I/O	I/O	P			PCI21	
46	N4	GND	DC in	GND	DC in	PWR	G			—	
47	L5	AD19	I/O	AD19	I/O	I/O	P			PCI21	
48	M5	AD18	I/O	AD18	I/O	I/O	P			PCI21	
49	N5	AD17	I/O	AD17	I/O	I/O	P			PCI21	
50	K6	AD16	I/O	AD16	I/O	I/O	P			PCI21	
51	L6	C/BE2#	I/O	C/BE2#	I/O	I/O	P			PCI21	
52	N6	FRAME#	I/O	FRAME#	I/O	I/O	P			PCI21	
53	M6	IRDY#	I/O	IRDY#	I/O	I/O	P			PCI21	
54	L7	TRDY#	I/O	TRDY#	I/O	I/O	P			PCI21	
55	N7	DEVSEL#	I/O	DEVSEL#	I/O	I/O	P			PCI21	
56	M7	STOP#	I/O	STOP#	I/O	I/O	P			PCI21	
57	K7	GND	DC in	GND	DC in	PWR	G			—	
58	N8	PERR#	I/O	PERR#	I/O	I/O	P			PCI21	
59	M8	SERR#	O	SERR#	O	O(OD)	P			PCI21	
60	L8	PAR	I/O	PAR	I/O	I/O	P			PCI21	
61	N9	C/BE1#	I/O	C/BE1#	I/O	I/O	P			PCI21	
62	K8	AD15	I/O	AD15	I/O	I/O	P			PCI21	
63	M9	AD14	I/O	AD14	I/O	I/O	P			PCI21	
64	N10	AD13	I/O	AD13	I/O	I/O	P			PCI21	
65	L9	AD12	I/O	AD12	I/O	I/O	P			PCI21	
66	M10	GND	DC in	GND	DC in	PWR	G			—	
67	N11	AD11	I/O	AD11	I/O	I/O	P			PCI21	
68	K9	AD10	I/O	AD10	I/O	I/O	P			PCI21	
69	L10	VCC_PCI	DC in	VCC_PCI	DC in	PWR	P			—	
70	N12	AD9	I/O	AD9	I/O	I/O	P			PCI21	
71	M11	AD8	I/O	AD8	I/O	I/O	P			PCI21	
72	L11	C/BE0#	I/O	C/BE0#	I/O	I/O	P			PCI21	
73	N13	AD7	I/O	AD7	I/O	I/O	P			PCI21	
74	M12	AD6	I/O	AD6	I/O	I/O	P			PCI21	
75	K10	AD5	I/O	AD5	I/O	I/O	P			PCI21	
76	M13	AD4	I/O	AD4	I/O	I/O	P			PCI21	
77	L12	GND	DC in	GND	DC in	PWR	G			—	

Pin No.	Ball No.	16-bit Card Interface		CardBus Card Interface		Pin Characteristics					Note
		Pin Name	Dir	Pin Name	Dir	Type	Pwr Rail	Pullup Pulldown 16 / CB		Drive	
78	K11	AD3	I/O	AD3	I/O	I/O	P			PCI21	
79	L13	AD2	I/O	AD2	I/O	I/O	P			PCI21	
80	K12	AD1	I/O	AD1	I/O	I/O	P			PCI21	
81	J10	AD0	I/O	AD0	I/O	I/O	P			PCI21	
82	K13	VCC_CORE	DC in	VCC_CORE	DC in	PWR	C			—	
83	J11	BVD1/ STSCHG#/ RI#	I	CSTSCHG	I	I(PU)/ I(PD)	A	PU	PD	—	3
84	J12	INPACK#	I	CREQ#	I	I(PU)	A	PU	PU	—	
85	J13	CDATA3	I/O	CAD0	I/O	I/O	A			8mA	1
86	H10	CDATA11	I/O	CAD2	I/O	I/O	A			8mA	1
87	H11	CDATA4	I/O	CAD1	I/O	I/O	A			8mA	1
88	H13	CDATA12	I/O	CAD4	I/O	I/O	A			8mA	1
89	H12	CDATA5	I/O	CAD3	I/O	I/O	A			8mA	1
90	G11	CDATA13	I/O	CAD6	I/O	I/O	A			8mA	1
91	G13	CDATA6	I/O	CAD5	I/O	I/O	A			8mA	1
92	G12	CDATA14	I/O	—	—	I/O	A			8mA	1
93	G10	CDATA7	I/O	CAD7	I/O	I/O	A			8mA	1
94	F13	GND	DC in	GND	DC in	PWR	G			—	
95	F12	CDATA15	I/O	CAD8	I/O	I/O	A			8mA	1
96	F11	CE1#	O	CC/BE0#	I/O	I/O	A			8mA	
97	E13	CE2#	O	CAD10	I/O	I/O	A			8mA	
98	F10	CADR10	O	CAD9	I/O	I/O	A			8mA	
99	E12	OE#	O	CAD11	I/O	I/O	A			8mA	
100	D13	IORD#	O	CAD13	I/O	I/O	A			8mA	
101	E11	CADR11	O	CAD12	I/O	I/O	A			8mA	
102	D12	IOWR#	O	CAD15	I/O	I/O	A			8mA	
103	C13	VCC_SLOT	DC in	VCC_SLOT	DC in	PWR	A			—	
104	E10	CADR9	O	CAD14	I/O	I/O	A			8mA	
105	D11	CADR17	O	CAD16	I/O	I/O	A			8mA	
106	B13	CADR8	O	CC/BE1#	I/O	I/O	A			8mA	
107	C12	CADR18	O	—	—	O(TS)	A			8mA	
108	C11	CADR13	O	CPAR	I/O	I/O	A			8mA	
109	A13	CADR19	O	—	—	O(TS)	A			8mA	
110	B12	CADR14	O	CPERR#	I/O	I/O (PU)	A		PU	8mA	2
111	D10	CADR20	O	CSTOP#	I/O	I/O (PU)	A		PU	8mA	2
112	A12	WE#	O	CGNT#	O	O(TS)	A			8mA	
113	B11	CADR21	O	CDEVSEL#	I/O	I/O (PU)	A		PU	8mA	2
114	C10	RDY/ IREQ#	I	CINT#	I	I(PU)	A	PU	PU	—	

Pin No.	Ball No.	16-bit Card Interface		CardBus Card Interface		Pin Characteristics					Note
		Pin Name	Dir	Pin Name	Dir	Type	Pwr Rail	Pullup Pulldown 16 / CB		Drive	
115	A11	CADR22	O	CTRDY#	I/O	I/O (PU)	A		PU	8mA	2
116	B10	GND	DC in	GND	DC in	PWR	G			—	
117	D9	CADR16	O	CCLK	O	O(TS)	A			CB	
118	A10	CADR23	O	CFRAME#	I/O	I/O	A			8mA	
119	C9	CADR15	O	CIRDY#	I/O	I/O (PU)	A		PU	8mA	2
120	B9	CADR24	O	CAD17	I/O	I/O	A			8mA	
109	A13	CADR19	O	—	—	O(TS)	A			8mA	
110	B12	CADR14	O	CPERR#	I/O	I/O (PU)	A		PU	8mA	2
111	D10	CADR20	O	CSTOP#	I/O	I/O (PU)	A		PU	8mA	2
112	A12	WE#	O	CGNT#	O	O(TS)	A			8mA	
113	B11	CADR21	O	CDEVSEL#	I/O	I/O (PU)	A		PU	8mA	2
114	C10	RDY/ IREQ#	I	CINT#	I	I(PU)	A	PU	PU	—	
115	A11	CADR22	O	CTRDY#	I/O	I/O (PU)	A		PU	8mA	2
116	B10	GND	DC in	GND	DC in	PWR	G			—	
117	D9	CADR16	O	CCLK	O	O(TS)	A			CB	
118	A10	CADR23	O	CFRAME#	I/O	I/O	A			8mA	
119	C9	CADR15	O	CIRDY#	I/O	I/O (PU)	A		PU	8mA	2
120	B9	CADR24	O	CAD17	I/O	I/O	A			8mA	
121	A9	CADR12	O	CC/BE2#	I/O	I/O	A			8mA	
122	D8	CADR25	O	CAD19	I/O	I/O	A			8mA	
123	C8	VCC_SLOT	DC in	VCC_SLOT	DC in	PWR	A			—	
124	A8	CADR7	O	CAD18	I/O	I/O	A			8mA	
125	B8	CADR6	O	CAD20	I/O	I/O	A			8mA	
126	C7	CADR5	O	CAD21	I/O	I/O	A			8mA	
127	A7	RESET	O	CRST#	O	O(TS)	A			4mA	
128	B7	CADR4	O	CAD22	I/O	I/O	A			8mA	
129	D7	WAIT#	I	CSERR#	I	I(PU)	A	PU	PU	—	
130	A6	CADR3	O	CAD23	I/O	I/O	A			8mA	
131	B6	GND	DC in	GND	DC in	PWR	G			—	
132	C6	CADR2	O	CAD24	I/O	I/O	A			8mA	
133	A5	REG#	O	CC/BE3#	I/O	I/O	A			8mA	
134	D6	CADR1	O	CAD25	I/O	I/O	A			8mA	
135	B5	BVD2/ SPKR#	I	CAUDIO	I	I(PU)	A	PU	PU	—	
136	A4	CADR0	O	CAD26	I/O	I/O	A			8mA	
137	C5	CDATA0	I/O	CAD27	I/O	I/O	A			8mA	1

Pin No.	Ball No.	16-bit Card Interface		CardBus Card Interface		Pin Characteristics					Note
		Pin Name	Dir	Pin Name	Dir	Type	Pwr Rail	Pullup Pulldown 16 / CB		Drive	
138	B4	CDATA8	I/O	CAD28	I/O	I/O	A			8mA	1
139	A3	CDATA1	I/O	CAD29	I/O	I/O	A			8mA	1
140	D5	CDATA9	I/O	CAD30	I/O	I/O	A			8mA	1
141	C4	CDATA2	I/O	—	—	I/O	A			8mA	1
142	A2	CDATA10	I/O	CAD31	I/O	I/O	A			8mA	1
143	B3	WP/ IOIS16#	I	CCLKRUN#	I/O	I/O (PU)	A		PU	8mA	2
144	C3	VCC_CORE	DC in	VCC_CORE	DC in	PWR	C			—	

Pin Type
I: Input Pin, O: Output Pin, I/O: Input Output Pin,
I(PU): Input Pin with Internal Pullup Resister,
I(PD): Input Pin with Internal Pulldown Resister,
I/O(PU): Input Output Pin with Internal Pullup Resister,
I/O(PD): Input Output Pin with Internal Pulldown Resister,
O(TS): Three State Output Pin, O(OD): Open Drain Output Pin

Power Rail
P: VCC_PCI, C: VCC_CORE, A: VCC_SLOT,
5: VCC_5V

Drive
PCI21: PCI2.1 Compliant,
CB: PCMCIA CardBus PC Card Compliant

Note
1: Pulldown is attached when PC Card Interface is configured as 16-bit Interface Mode.
2: Pullup is attached when PC Card Interface is configured as a CardBus Interface Mode.
3: Pullup or Pulldown is configured according to the type of a card inserted.

3.3 Pin Functions Outline & Description

In this chapter, the detailed signal pins in RL5C475 are explained. Every signal is divided according to their relational interface.

Card Interface signal pin is multi-functional pin. Card Interface mode is configured automatically by the card insertion ; CardBus card or 16-bit card. And the pin function is redefined again.

mark means the signal is on either active or asserted when the signal is low-level. Otherwise, no-mark means the signal is asserted when the signal is high-level.

The following the notations are used to describe the signal type.

IN	Input Pin
OUT	Output Pin
OUT(TS)	Three State Output Pin
OUT(OD)	Open Drain Output Pin
I/O	Input Output Pin
I/O(OD)	Input Output Pin (Output is Open Drain)
s/h/z	Sustained Tri-State is an active low tri-state signal owned and driven by one and only one agent at a time. The agent that drives an s/h/z pin low must drive it high for at least one clock before letting it float. A new agent cannot start driving a s/h/z signal any sooner than one clock after the previous owner tri-state is.

3.4 PCI Local Bus interface

Pin Name	Type	Description
		PCI Bus Interface Pin Descriptions
PCICLK	IN	***PCI CLOCK:*** PCICLK provides timing for all transactions on PCI. All other PCI signals are sampled on the rising edge of PCICLK.
CLKRUN#	I/O	***PCI CLOCK RUN:*** This signal indicates the status of PCICLK and an open drain output to request the starting or speeding up of PCICLK. This pin complies with Mobile PCI specification. This signal has no meaning for 16bit card. Tie to GND if not used.
PCIRST#	IN	***PCI RESET:*** This input is used to initialize all registers, sequences and signals of the RL5C475A to their rest states. All of the outputs of the RL5C475A will be tri-stated during PCIRST is asserted.
AD[31:0]	I/O	***ADDRESS AND DATA:*** Address and Data are multiplexed on the same PCI pins.
C/BE[3:0]#	I/O	***BUS COMMAND AND BYTE ENABLES:*** Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data.
PAR	I/O	***PARITY:*** Parity is even parity across AD[31:0] and C/BE[3:0]#. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. The master drives PAR for address and write data phases; the target drives PAR for read data phases.
FRAME#	I/O s/h/z	***CYCLE FRAME:*** This signal is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has complete.
TRDY#	I/O s/h/z	***TARGET READY:*** This signal indicates the initialing agent's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31:0]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted both IRDY# and TRDY# are asserted together.
IRDY#	I/O s/h/z	***INITIATOR READY:*** This signal indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31:0]. During a read, it indicates the target is prepared to accept data. Wait cycles are inserted both IRDY# and TRDY# are asserted together.
STOP#	I/O s/h/z	***STOP:*** This signal indicates the current target is requesting the master to stop the current transaction.
IDSEL	IN	***INITIALIZATION DEVICE SELECT:*** This signal is used as a chip select during configuration read and write transactions.
DEVSEL#	I/O s/h/z	***DEVICE SELECT:*** When actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
PERR#	I/O s/h/z	***PARITY ERROR:*** This signal is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The RL5C475A drives this output active "low" if it detects a data parity error during a write phase.
SERR#	OUT(OD)	***SYSTEM ERROR:*** This signal is pure open drain. The RL5C475A actively drives this output for a single PCI clock when it detects an address parity error on either the primary bus or the secondary bus.
REQ#	OUT(TS)	***REQUEST:*** This signal indicates to the arbiter that the RL5C475A desires use of the bus. This is a point to point signal.
GNT#	IN	***GRANT:*** This signal indicates the RL5C475A that access to the bus has been granted. This is a point to point signal.

3.5 System Interrupt Signals

Pin Name	Type	Description
		System Interrupt Pin Descriptions
INTA#	OUT(OD)	***PCI INTERRUPT REQUEST A:*** This signal indicates a programmable interrupt request generated from the card socket A interface. This signal is connected PCI bus INTA# interrupt line.
IRQ3/GPIO0 IRQ4/GPIO1 IRQ5/GPIO2 IRQ7/GPIO3 IRQ9/SRIRQ# IRQ10 IRQ11 IRQ12/ LEDOUT IRQ14 IRQ15/ ZVEN#	OUT(TS)	***SYSTEM INTERRUPT REQUEST IRQ 3-15:*** These signals indicate the interrupts requests from one of the cards and are connected to the ISA bus IRQx signal. IRQ12 is reassigned as an LED output when LED enable bit in ATA control register is set to one. When Serial IRQ Enable bit in Misc Control register is set to one, IRQ9 is reassigned as SRIRQ# signal, at the same time IRQ15 is reassigned as ZVEN# signal ; ZV port buffer control signal. When Serial IRQ signal is enabled, IRQ3,4,5 and 7 are assigned as GPIO (General Purpose I/O) pins. These are input/output pins determined by user without effect on the controller transaction.
RI_OUT#/ PME#	OUT(TS)	***RING INDICATE OUTPUT:*** When 16-bit card is inserted, this signal is assigned as RI_OUT# from a socket's RI# input when Ring Indicate Enable bit in Interrupt and General control register is set to one. When 32bit card is inserted, this signal indicates the inverted state of CSTSCHG signal when WAKEUP Enable bit in Socket Wakeup Control register is set to one. ***POWER MANAGEMENT EVENT:*** When PME_En bit in Power Management Control/Status register is set or when Power Status is set to any state mode except D0, this signal is assigned as PME#.

3.6 16-bit PC Card Interface Signals

Pin Name	Type	Description
16-bit PC Card Interface Pin Descriptions		
CDATA[15:0]	I/O	***16-bit Card DATA BUS SIGNALS [15:0]:*** Input buffer is disabled when the card socket power supply is off or card is not inserted.
CADR[25:0]	OUT(TS)	***16-bit Card ADDRESS BUS SIGNALS [25:0]:***
IOR#	OUT(TS)	***16-bit Card I/O READ:***
IOW#	OUT(TS)	***16-bit Card I/O WRITE:***
OE#	OUT(TS)	***16-bit Card OUTPUT ENABLE:***
WE#	OUT(TS)	***16-bit Card WRITE ENABLE:***
CE1#	OUT(TS)	***16-bit Card CARD ENABLE 1:***
CE2#	OUT(TS)	***16-bit Card CARD ENABLE 2:***
REG#	OUT(TS)	***16-bit Card ATTRIBUTE MEMORY SELECT:*** Memory access is limited to Attribute memory when this signal is “low”. During normal access for I/O, this signal is kept “low” and “high” for DMA transfers.
READY/ IREQ#	IN	***16-bit Card READY/BUSY or INTERRUPT REQUEST:*** This signal has two different functions. READY/BUSY# input on the memory PC card, and IREQ# input on the I/O card.
WP/ IOIS16#	IN	***16-bit Card WRITE PROTECT or CARD IS 16-BIT PORT:*** This signal has two different functions. Write Protect Switch input on the memory PC card, and IOIS16 input on the I/O card.
RESET	OUT(TS)	***16-bit Card CARD RESET:***
WAIT#	IN	***16-bit Card BUS CYCLE WAIT:***
BVD1/ STSCHG#/ RI#	IN	***16-bit Card BATTERY VOLTAGE DETECT 1 or STATUS CHANGE:*** This signal has three different functions. The battery voltage detect input 1 on the memory PC card, and Card Status Change#/Ring Indicate# input on the I/O card.
BVD2/ SPKR#/ LED	IN	***16-bit Card BATTERY VOLTAGE DETECT 2 or DIGITAL AUDIO or LED INPUT:*** This signal has three different functions. The battery voltage detect input 2 on the memory PC card, and SPEAKER# input or LED input on the I/O card.
INPACK#	IN	***16-bit Card INPUT ACKNOWLEDGE:***
CD1#	IN	***16-bit Card CARD DETECT 1:*** CD[2:1]# pins are used to detect the card insertion. CD[2:1]# pins are used in conjunction with VS[2:1]# to decode card type information.
CD2#	IN	***16-bit Card CARD DETECT 2:*** CD[2:1]# pins are used to detect the card insertion. CD[2:1]# pins are used in conjunction with VS[2:1]# to decode card type information.
VS1	I/O	***16-bit Card CARD VOLTAGE CAPABILITY SENSE 1:*** VS[2:1]# pins are used in conjunction with CD[2:1] to decode card type information.
VS2	I/O	***16-bit Card CARD VOLTAGE CAPABILITY SENSE 2:*** VS[2:1]# pins are used in conjunction with CD[2:1]# to decode card type information.

3.7 CardBus PC Card Interface Signals

Pin Name	Type	Description
CardBus PC Card Interface Pin Descriptions		
CCLK	OUT(TS)	***CardBus Clock:*** This signal provides timing for all transactions on the PC Card Standard 95 interface and it is an input to every PC Card Standard 95 device. All other CardBus PC Card signals, except CRST# (upon assertion), CCLKR, CCLKRUN#, CINT#, CSTSCHG, CAUDIO, CCD[2:1]#, and CVS[2:1], are sampled on the rising edge of CCLK, and all timing parameters are defined with respect to this edge.
CCLKRUN#	I/O s/h/z	***CardBus Clock Run:*** This signal is used by cards to request starting (or speeding up) clock ; CCLK. CCLKRUN# also indicates the clock status. For PC cards, CCLKRUN# is an open drain output and it is also an input. The RL5C475A indicates the clock status of the primary bus to the CardBus card.
CRST#	OUT(TS)	***CardBus Card Reset:*** This signal is used to bring CardBus Card specific registers, sequencers and signals to a consistent state. Anytime CRST# is asserted, all CardBus card output signals will be driven to their begin state.
CAD[31:0]	I/O	***CardBus Address/Data:*** These signals are multiplexed on the same CardBus card pins. A bus transaction consists of an address phase followed by one or more data phases. CardBus card supports both read and write bursts. CAD[31:0] contain a physical address (32 bits). For I/O, this is a byte address ; for configuration and memory it is a DWORD address. During data phases, CAD[7:0] contain the east significant byte(LSB) and CAD[31:24] contain the most significant byte(MSB). Write data is stable and valid when CIRDY# is asserted and read data is stable and valid when CTRDY# is asserted. Data is transferred during those clocks where both CIRDY# and CTRDY# are asserted.
CC/BE[3:0]#	I/O	***CardBus Command/Bye Enables:*** These signals are multiplexed on the same CardBus card pins. During the address phase of a transaction, CC/BE[3:0]# define the bus command. During the data phase, CC/BE[3:0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. CC/BE[0]# applies to byte 0 (LSB) and CC/BE[3]# applies to byte 3 (MSB).
CPAR	I/O	***CardBus Parity:*** This signal is even parity across CAD[31:0] and CC/BE[3:0]#. Parity generation is required by all CardBus card agents. CPAR is stable and valid clock after either CIRDY# is asserted on a write transaction or CTRDY# is asserted on a read transaction. Once CPAR is valid, it remains valid until one clock after the completion of the current data phase. (CPAR has the same timing as CAD[31:0] but delayed by one clock.) The master drives CPAR for address and write data phases ; the target drives CPAR for read data phases.
CFRAME#	I/O s/h/z	***CardBus Cycle Frame*****:** This signal is driven by the current master to indicate the beginning and duration of a transaction. CFRAME# is asserted to indicate that a bus transaction is beginning. While CFRAME# is asserted, data transfers continue. When CFRAME# is deasserted, the transaction is in the final data phase.
CIRDY#	I/O s/h/z	***CardBus Initiator Ready:*** This signal indicates the initiating agent's(bus master's) ability to complete the current data phase of the transaction. CIRDY# is used in conjunction with CTRDY#. A data phase is completed on any clock both CIRDY# and CTRDY# are sampled asserted. During a write, CIRDY# indicates that valid data is present on CAD[31:0]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both CIRDY# and CTRDY# are asserted together.
CTRDY#	I/O s/h/z	***CardBus Target Ready:*** This signal indicates the agent's(selected target's) ability to complete the current data phase of the transaction. CTRDY# is used in conjunction with CIRDY#. A data phase is completed on any clock both CTRDY# and CIRDY# are sampled asserted. During a read, CTRDY# indicates that valid data is present on CAD[31:0]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both CIRDY# and CTRDY# are asserted together.
CSTOP#	I/O s/h/z	***CardBus Stop:*** This signal indicates the current target is requesting the master to stop the current transaction.
CDEVSEL#	I/O s/h/z	***CardBus Device Select:*** This signal indicates the driving device has decoded its address as the target of the current access when actively driven. As an input, CDEVSEL# indicates whether any device on the bus has been selected.
CREQ#	IN	***CardBus Request:*** This signal indicates to the arbiter that this agent desires use of the bus. Every master has its own CREQ#.

Pin Name	Type	Description
CardBus PC Card Interface Pin Descriptions (Continued)		
CGNT#	OUT	***CardBus Grant:*** This signal indicates to the agent that access to the bus has been granted. Every master has its own CGNT#.
CPERR#	I/O s/h/z	***CardBus Parity Error:*** This signal is only for the reporting of data parity errors during all CardBus Card transactions except a Special Cycle. An agent cannot report a CPERR# until it has claimed the access by asserting CDEVSEL# and completed a data phase.
CSERR#	IN	***CardBus System Error:*** This signal is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result could be catastrophic.
CINT#	IN	***CardBus Interrupt Request:*** This signal is an input signal from CardBus card. It is level sensitive, and asserted low (negative true), using an open drain output driver. The assertion and deassertion of CINT# is asynchronous to CCLK.
CSTSCHG	IN	***CardBus Card Status Change:*** This signal is an input signal used to alert the system to changes in the READY, WP, or BVD[2:1] conditions of the card. It is also used for the system and/or CardBus card interface Wake up. CSTSCHG is asynchronous to CCLK.
CAUDIO	IN	***CardBus Card Audio:*** This signal is a digital audio input signal from a CardBus Card to the system's speaker. CAUDIO has no relationship to CCLK.
CCD1#	IN	***CardBus Card Detect 1:*** CCD[2:1]# pins are used to detect the card insertion. CCD[2:1]# pins are used in conjunction with CVS[2:1]# to decode card type information.
CCD2#	IN	***CardBus Card Detect 2:*** CCD[2:1]# pins are used to detect the card insertion. CCD[2:1]# pins are used in conjunction with CVS[2:1]# to decode card type information.
CVS1	I/O	***CardBus Card Voltage Sense 1:*** CVS[2:1]# pins are used in conjunction with CCD[2:1]# to decode card type information.
CVS2	I/O	***CardBus Card Voltage Sense 2:*** CVS[2:1]# pins are used in conjunction with CCD[2:1]# to decode card type information.

3.8 Socket Power Control Signals

Pin Name	Type	Description
		Socket Power Control Signal Descriptions
VCC5EN#	OUT	***VCC 5V ENABLE:***
VCC3EN#	OUT	***VCC 3.3V ENABLE:***
VPPEN0	OUT	***VPP ENABLE 0:***
VPPEN1	OUT	***VPP ENABLE 1:***

3.9 Audio · General Signals

Pin Name	Type	Description
		Audio Pin Descriptions
SPKROUT#/ HWSPND#	OUT(TS)	***SPEAKER OUTPUT:*** This signal is a digital audio output from SPKR#. When Hardware suspend enable bit in Misc Control register is set to one, this pin works as a Hardware Suspend# input. This signal must be pulled up with 100K register. When Serial IRQ mode is set, HWSPND# must be asserted after Serial IRQ mode on the chip-set has been deasserted. When Hardware Suspend mode is off, HWSPND# must be deasserted before Serial IRQ mode is enabled.
LED#	OUT	***LED OUTPUT:*** This signal outputs “Low” when CardBus Card is accessed. Setting LED Polarity bit in Misc Control register is enabled to output “High” on accessing.

3.10 Power and GND

Pin Name	Type	Description
		Power Pin Descriptions
VCC_PCI	PWR	***PCI VCC :*** Power Supply pins for PCI interface signals. This pin can be powered at either 3.3V or 5V.
VCC_CORE	PWR	***CORE VCC :*** Power Supply pins for the internal core logic. This pin must be powered at 3.3V only.
VCC_SLOT	PWR	***SLOTA VCC :*** Power Supply for Card socket A. This pin can be powered at either 3.3V or 5V.
VCC_5V	PWR	***5V VCC :*** This supply pin is connected to 5V. In systems where 5V is not available, this pin is connected to 3.3V.
GND	PWR	***GND :***

4 FUNCTIONAL DESCRIPTION

4.1 Device Configuration

5C475 supports PCI-CardBus Bridge Interface functions for PC Card socket with three kind of register spaces. Logically the 5C475 looks to the primary PCI as a separate secondary bus residing in a single device. The socket has its own register spaces as follows.

4.1.1 PCI Configuration Register Space

PCI Configuration registers are used to control the basic operations, as a setting of PCI device and a status control, in the 5C475. The 5C475 implements a 256 bytes configuration space an each socket. The first 64bytes in a socket configuration space adhere to a predefined header format. The remaining 192 bytes of the configuration space is used for a socket control purpose. The 5C475 configuration space is accessible only from the primary PCI bus. No other interfaces respond to configuration cycles.

4.1.2 CardBus (32-bit) Card Control Register Space

CardBus Card Control registers are used to manage status changed events, remote wakeup events and status information about the PC Card in the socket. These registers are used for PC Card-32 as well as PC Card-16. PC Card Control Register Base Address register points to the 4 Kbyte memory mapped I/O space that contains both the PC Card-32 and PC Card-16 Status and Control registers. Socket Status/Control Registers for Card-32 are placed in the lower 2Kbyte of the 4Kbyte and start at offset 000h.

4.1.3 16-bit Card Control Register Space

Socket Status/Control Registers for PC Card-16 are placed in the upper 2Kbyte of the 4Kbyte pointed by the PC Card Control Register Base Address register and start at offset 800h.

4.1.4 16-bit Legacy Port

Legacy mode allows all 16-bit Card Control registers to be accessed through the index/data port at I/O address 3E0/3E2 in order to maintain the backward compatibility with Intel 82365 compatibles like Ricoh RF5C396/366.

4.2 CardBus Card Configuration Mechanism

CardBus Card supports the configuration spaces following the PCI specifications. CardBus Card is also configured by the host. The 5C475 supports functions of changing Type 0 PCI configuration command into Type 1 PCI configuration command and transferring them.

4.3 Address Window and Mapping Mechanism

The 5C475 supports one PCI-Card Bridge Interface functions and determines if it is CardBus Card or 16-bit Card automatically on inserting a card. Each interface can be set independently.

On CardBus Card interface, the transaction is forwarded by two I/O windows, two memory map I/Os and a prefetchable memory window. CardBus Card address and PCI system address use a flat address in common. So the address range specified by a base register and a limit register is forwarded from PCI to CardBus Card.

And also, the 5C475 supports CardBus Master, so the transfer transaction from CardBus Card interface to PCI interface or to the other card interface is supported. The transaction out of an address range specified by a base register and a limit register is passed to PCI bus.

On 16-bit Card interface, the transaction is transferred by two I/O windows and five memory windows set on 16-bit Card Status Control registers which are compatible with PCIC. The transfer is permitted only from PCI interface to CardBus.

4.3.1 ISA mode

The 5C475 supports the ISA mode. Setting ISA enable bit of Bridge Control register enables ISA mode. This mode applies only to addresses that are enabled by the I/O Base and Limit registers and are also in the first 64K Byte of PCI I/O space. When set, the 5C475 will block forwarding from PCI to CardBus I/O transactions addressing the last 768bytes in each 1K byte block. In the opposite direction(CardBus to PCI) I/O transaction will be forwarded if they address the last 768 bytes in each 1K block.

4.3.2 VGA mode

The 5C475 supports the VGA mode. When the VGA enable bit of Bridge Control register is set, the 5C475 will forward transactions from PCI to CardBus I/F in the following ranges.

Memory address :	0A0000h to 0BFFFFh
I/O address :	AD[9:0] = 3B0h to 3BBh, and 3C0h to 3DFh (inclusive of ISA address aliases - AD[15:10] are not decoded.)

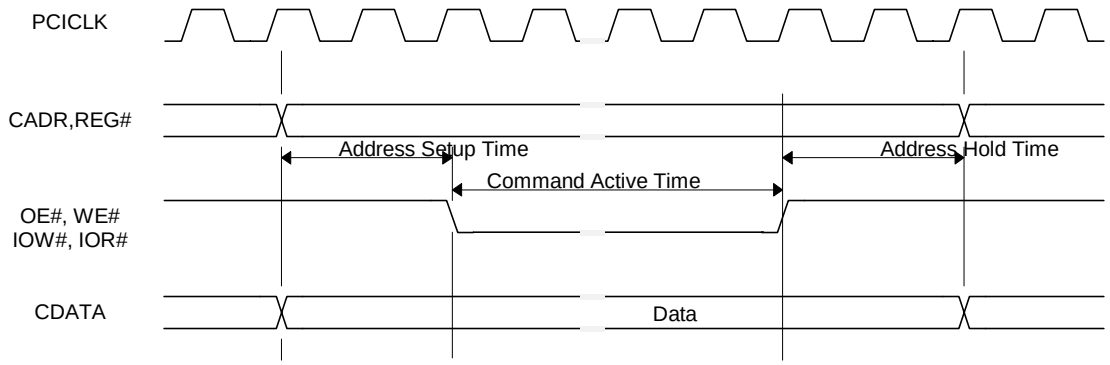
And also, the 5C475 will forward only write transaction to the VGA Palette register in the following ranges.

Palette address :	AD[9:0] = 3C6h, 3C8h, and 3C9h (inclusive of ISA address aliases - AD[15:10] are not decoded.)

4.4 16-bit Card Interface Timing Control

The 5C475 generates the address, data, and command timing necessary to 16-bit Card interface. Each timing is set in a timer granularity of PCI clock as shown below. When 16-bit I/O enhanced Timing or 16-bit Memory Enhanced Timing bit in each socket control register space is cleared, the default timing is selected regardless of the I/O Win 0-1 Enhanced Timing bit or Memory Enhanced Timing bit. Default timing will be selected when the value smaller than the minimum value is set.

16-bit Card Signal Timing Example



Symbol	Parameter	Min	Max	Default	Unit
	I/O Read/ Write				
Tsu	Address Setup Time	2	7	3	PCI Clocks (Typ=30ns)
Tpw	Command Active Time	3	31	6	PCI Clocks (Typ=30ns)
Thl	Address Hold Time	1	7	1	PCI Clocks (Typ=30ns)
	Memory Read/ Write				
Tsu	Address Setup Time	1	7	3 (4) Note 1	PCI Clocks (Typ=30ns)
Tpw	Command Active Time	3	31	6 (8or18) Note 2	PCI Clocks (Typ=30ns)
Thl	Address Hold Time	1	7	1(2) Note1	PCI Clocks (Typ=30ns)

Note1 : 4(2)PCI clocks for 3.3v card attribute memory access.

Note2 : 8 PCI clocks for 5v card attribute memory access.
18 PCI clocks for 3.3v card attribute memory access.

4.5 PCI Buffers

The 5C475 has data buffers, address buffers, and command buffers between the primary PCI bus and the secondary CardBus in order to maintain the high speed data transferring. A 8-DWORD buffer allows Posting Write Data and Prefetching Read Data from PCI bus to CardBus as well as from CardBus to PCI bus. Posting of write data is permitted when either Memory Write or Memory Write and Invalidate commands are used for transactions that cross the 5C475 in either direction. In other words, writing buffers are not available during the I/O Write and Configuration Write transactions. The 5C475 prefetches data when the transaction uses the Memory Read Line or Memory Read Multiple command.

4.6 Error Support

4.6.1 Parity Error

The 5C475 supports both parity generation and checking in both address and data phases on both the primary PCI bus and the secondary CardBus. The 5C475 asserts SERR# when an address parity error occurs during the bus transaction on either PCI bus or CardBus. When the 5C475 detects a data parity error the bad data and bad parity will be passed on to the opposite interface if possible and PERR# is asserted. This will enable the parity error recovery mechanisms outlined in the PCI Local Bus Specification. If CSERR# is asserted on CardBus interface, the 5C475 forwards a SERR# indication on the CardBus to the primary PCI bus.

4.6.2 Master Abort

When the master abort occurs at the destination, the 5C475 behaves in two ways. One is ISA compatible. (returns all ones during a read. The data will be discarded during a write.) The other way is to assert SERR#.

4.6.3 Target Abort

When the target abort occurs at the opposite side, the 5C475 communicates the error as a target abort to the origination master if possible. But, if can not, the 5C475 will assert SERR# and communicate the error to the system.

4.6.4 CardBus System Error

When CSERR# is asserted on the secondary CardBus interface, the 5C475 always asserts SERR# on the primary PCI interface and communicate the error to the system.

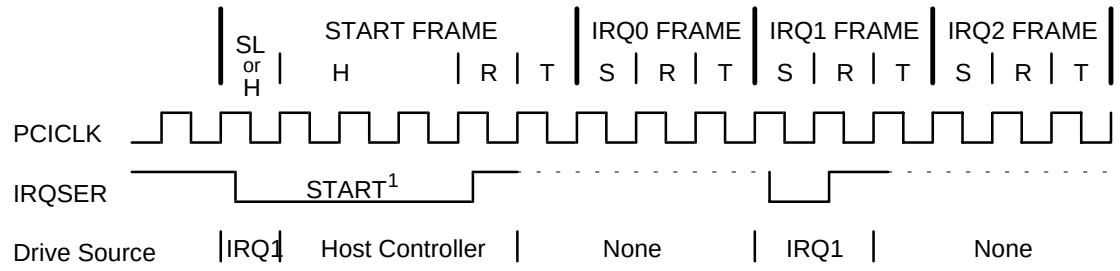
4.7 Interrupts

The 5C475 supports PCI interrupt signals INTA# as well as ISA interrupt signals IRQn. Setting IRQ-ISA enable bit of Bridge Control register enables the IRQn routing register for PC Card-16. ISA IRQn interface is programmable to either positive edge mode or level mode. On the other hand, PCI interrupt signals are open drain outputs. RI_OUT# can be reassigned as an interrupt signal for the purpose of the remote wakeup.

In addition to primary interrupt functions, the 5C475 supports Serialized IRQ. IRQ9 is reassigned as SRIRQ# by setting SRIRQ Enable bit (bit7) on the Misc Control register. SRIRQ# (Serialized IRQ) output is a Wire-OR structure that simply passes the state of one or more device's IRQ to the host controller. The transfer can be initiated by either a device or the host controller. A transfer, called an IRQSER Cycle, consists of three frame types: one Start Frame, several IRQ/Data Frames, and one Stop frame. The 5C475 can insert the frames of INTA#, INTB#, INTC#, and INTD# (PCI Interrupt signals) following IOCHK# frame if SR_PCIINT_Disable bit is zero in the Misc control register. And also, setting SR_PCI_INT_Select bits(bit4,3) of Misc Control register enable to select which one of INTA-D. The default is INTA.

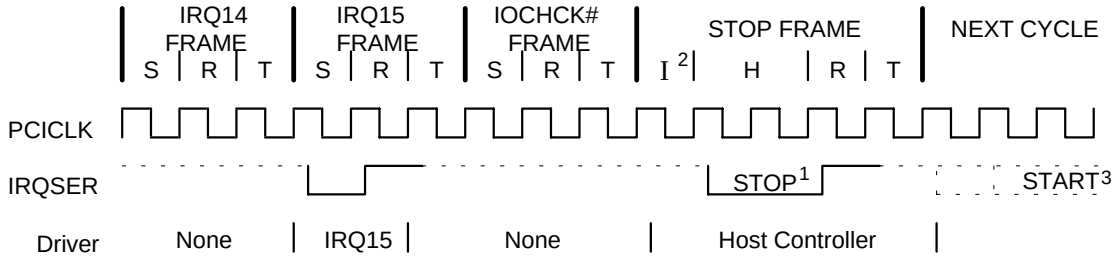
The Start Frame timing and the Stop Frame timing are as follows.

Start Frame timing with source sampled a low pulse on IRQ1



1. Start Frame pulse can be 4-8 clocks wide.

Stop Frame Timing with Host using 17 IRQSER sampling period



H=Host, SL=Slave Control, R=Recovery, T=Turn-around, S=Sample

1. Stop pulse are 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.
2. There may be none, one or more Idle states during the Stop Frame.
3. The next IRQSER cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.

All cycle uses PCICLK as its clock source. There are two modes of operation for the IRQSER Start Frame : Quiet (Active) mode and Continuous (Idle) mode. In Quiet (Active) mode any device can initiate a Start Frame, and in Continuous (Idle) mode only Host Controller can initiate a Start Frame. These modes change on the inside automatically by monitoring the Stop pulse wide in a Stop Frame. On the reset, the default is Continuous (Idle) mode.

IRQSER Sampling Periods		
IRQ/Data Frame	**Signal Sampled**	**# of clocks past Start**
1	IRQ0	2
2	IRQ1	5
3	SMI#	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47
17	IOCHCK#	50
18	INTA#	53
19	INTB#	56
20	INTC#	59
21	INTD#	62
32:22	Unassigned	95

4.8 Card Type Detection

If once a valid insertion is detected, the socket state machine of the 5C475 starts to interrogate the PC Card to determine if it is a PC Card Standard 95 or 16-bit PC Card. The 5C475 supports VCC values of 5V, 3.3V and combination of them at the socket interface. Card type can be known by reading the Socket Present State register.

CD2#	CD1#	VS2#	VS1#	Card Type		
				Key	Interface	Voltage
ground	ground	open	open	5V	16bit PC Card	5V
ground	ground	open	ground	5V	16bit PC Card	5V and 3.3V
ground	ground	ground	ground	5V	16bit PC Card	5V, 3.3V and X.XV
ground	ground	open	ground	LV	16bit PC Card	3.3V
ground	connect to CVS1	open	connect to CCD1#	LV	CardBus PC Card	3.3V
ground	ground	ground	ground	LV	16bit PC Card	3.3V and X.XV
connect to CVS2	ground	connect to CCD2#	ground	LV	CardBus PC Card	3.3V and X.XV
connect to CVS1	ground	ground	connect to CCD2#	LV	CardBus PC Card	3.3V, X.XV and X.XV
ground	ground	ground	open	LV	16bit PC Card	X.XV
connect to CVS2	ground	connect to CCD2#	open	LV	CardBus PC Card	X.XV
ground	connect to CVS2	connect to CCD1#	open	LV	CardBus PC Card	X.XV and Y.YV
connect to CVS1	ground	open	connect to CCD2#	LV	CardBus PC Card	Y.YV
ground	connect to CVS1	ground	connect to CCD1#	reserved		
ground	connect to CVS2	connect to CDD1#	ground	reserved		

4.9 Mixed Voltage Operation

The 5C475 has 4 independent power nets. PCI Bus interface can be powered at either 3.3V or 5V. The PC card interfaces of the 5C475 is independently powered so that one card can be powered at 5V while the other is powered at 3.3V. This mechanism allows 5C475 to maintain the backward compatibility with PCMCIA2.1 compliant cards (R2 card). No external level shifters are required. The core logic is powered only at 3.3V.

4.10 Power Management

The 5C475 implements two kinds of power management, software suspend mode and hardware suspend mode, in order to reduce the power dissipation on the suspend, in addition to the adoption of circuit to reduce the power consumption when power on. The software suspend mode conforms to the ACPI (Advanced Configuration and Power Interface) specification and the PCI Bus Power Management Standard. The 5C475, as a PCI device, implements four power states of D0, D1, D2, D3hot, and D3cold. Each power states is the following.
The power management events for the 5C475 and their sources are listed below. The interrupt from the following Events is disabled when the power state is selected except D0, because only PME# is enabled to assert.

Event	Source
Card Detect Change	5C475
Ready/Busy Change	card
Battery Warning	card
Ring Indicate (Card Status Change)	card

D0	the maximum powered state. All PCI transactions are acceptable.
D1	Only the PCI Configuration Space access is allowed while the power and clock are provided. CardBus CLK is output.
D2	Only the PCI Configuration Space access is allowed while the power and clock are provided. CardBus CLK is stopped by the protocol of CLKRUN.
D3hot	Only the PCI Configuration Space access is allowed while the power and clock are provided. CardBus CLK is stopped compulsorily. If CardBus card is inserted, CardBus RESET# is asserted at the same time this state is set. When the function is brought back to the D0 state, the reset is automatically performed regardless of the assertion of PCIRST#. PCI interface is disabled when reset. CardBus interface is reset by the assertion of CRST# on CardBus card or RESET on 16bit card.
D3cold	PCI-CardBus Bridge defines D3cold state is to change from Vcc to the auxiliary power source. The 5C475 supports power management events from D3cold with the auxiliary power source. The 5C475 can generate PME# even in D3cold state without PCI clock if the event source is Card Detect Change or Ring Indicate.

The following registers are not initialized by either PCIRST# or the reset generated by the power state transition from D3 to D0 as long as the power state is D3 and PME Enable bit is set to ”1”. (PME_Context)

Address	Register Name	Bit
000h	Socket Event	[3:0]
004h	Socket Mask	[3:0]
008h	Socket Present State	[11,10,5,4]
010h	Socket Control	[6:4]
802h	Power Control	[7:2]
804h	Card Status Change	[3:0]
805h	Card Status Change Interrupt Configuration	[3:0]
82Fh	Misc Control 1	[0]
DEh	Power Management Capabilities	[15]
E0h	Power Management Control/Status	[15, 8]

And also, each bit of the following registers is initialized under the each different conditions.

1. It is initialized by only PCIRST# independently of the power state.

Address	Register Name	Bit
82h	Misc Control	[15:0]

2. It is initialized by PCIRST# when the power state is selected except D3

Address	Register Name	Bit
40h	Subsystem Vender ID	[15:0]
42h	Subsystem ID	[15:0]

*The rest of bits(except the above bits) are initialized by the internal reset or the assertion PCIRST# under no conditions.

In the software suspend mode, when the card is inserted, the interface signals on sockets are kept to the following levels.

CardBus : CCLK=low, CPAR=low, CAD=high or low, CCBE#=high or low, CRST#= low, CGNT#=high

16-bit : CDATA=hi-z, CADR=low

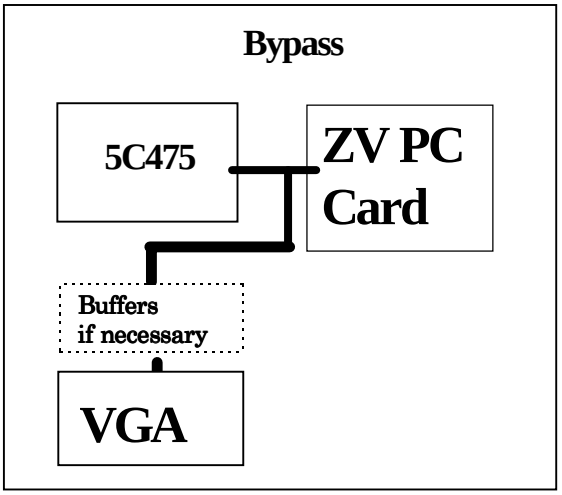
In addition to the Operating system-directed power management like ACPI, the 5C475 supports CLKRUN# and CCLKRUN# protocol and it results in a clock stopped and a slow clock. Therefore, it is possible to reduce the power consumption. The state of the card interface signals is the same as the software suspend mode. The hardware suspend mode is enabled when HWSPND# is asserted by setting Hardware Suspend# Enable bit of MISC Control register to one. In this mode, SPKOUT pin is reassigned as HWSPND# pin. Once HWSPND# is asserted, all PCI bus interface signals are disabled, and VCC_PCI can be powered off. PCIRST# is not accepted as long as HWSPND# is asserted low.

4.11 Reset Event

Anytime PCIRST# is asserted, all 5C475 internal state machines are reset and all registers are set to their default values. The default values of each registers are described in each register description.

4.12 ZV port Interface

The 5C475 has Bypass type ZV port interface. On 16-bit interface, when ZV port Enable bit of Misc Control 1 (82Fh) is enabled, CARDR[25:4], IOIS16#, INPACK#, SPKR# are assigned to ZV port input signal as shown in the diagram of nest page.
The 5C475 has no on chip buffer for ZV port interface. So if ZV port is enabled, the signals for ZV port such as CADR[25:4] will be “Hi-z” or “Input disable” and will be reconfigured as ZV port interface. The 5C475 outputs the control signal for the external buffer only when S_IRQ was enabled.



16 bit interface Signal Name	ZV Port Interface Signal Name	ZV Port card I/O [1]	Comments
A10	**HREF**	O	Horizontal Sync to ZV Port
A11	**VSYNC**	O	Vertical Sync to ZV Port
A9	**Y0**	O	Video Data to ZV Port YUV:4:2:2 format
A8	**Y2**	O	Video Data to ZV Port YUV:4:2:2 format
A13	**Y4**	O	Video Data to ZV Port YUV:4:2:2 format
A14	**Y6**	O	Video Data to ZV Port YUV:4:2:2 format
A16	**UV2**	O	Video Data to ZV Port YUV:4:2:2 format
A15	**UV4**	O	Video Data to ZV Port YUV:4:2:2 format
A12	**UV6**	O	Video Data to ZV Port YUV:4:2:2 format
A7	**SCLK**	O	Audio SCLK PCM Signal
A6	**MCLK**	O	Audio MCLK PCM Signal
A[5::4]	**RESERVED**	RFU	Put in three state by Host Adapter No connection in PC Card
A[3::0]	**ADDRESS[3::0]**	I	Used for accessing PC Card
IOIS16#	**PCLK**	O	Pixel Clock to ZV Port
A17	**Y1**	O	Video Data to ZV Port YUV:4:2:2 format
A18	**Y3**	O	Video Data to ZV Port YUV:4:2:2 format
A19	**Y5**	O	Video Data to ZV Port YUV:4:2:2 format
A20	**Y7**	O	Video Data to ZV Port YUV:4:2:2 format
A21	**UV0**	O	Video Data to ZV Port YUV:4:2:2 format
A22	**UV1**	O	Video Data to ZV Port YUV:4:2:2 format
A23	**UV3**	O	Video Data to ZV Port YUV:4:2:2 format
A24	**UV5**	O	Video Data to ZV Port YUV:4:2:2 format
A25	**UV7**	O	Video Data to ZV Port YUV:4:2:2 format
INPACK#	**LRCLK**	O	Audio LRCLK PCM signal
SPKR#	**SDATA**	O	Audio PCM Data signal

ZV Port Interface Pin Assignments

1. "I" indicates signal is input to PC Card, "O" indicates signal is output from PC Card.

4.13 Subsystem ID , Subsystem Vendor ID

The 5C475 supports Subsystem ID and Subsystem Vendor ID to meet PC98 Design Requirements. It is possible to write into Subsystem ID register and Subsystem Vendor ID register from the system through BIOS by setting Subsystem ID Write Enable bit (Misc Control 82-83h bit6).

4.14 GPIO

IRQ3, 4, 5 and 7 pins work as GPIO (General Purpose I/O) pin when SRIRQ# is configured. User can change each GPIO pin to either Input or Output by setting I/O control bits on GPIO register (83Ah). The default is Input mode. GPIO pin must be pull-up in outside in spite of use, or no use.

4.15 Notation

The following table shown the notation used in the register description.

NS	**not supported :** is used to indicate that registers and bits are not supported in 5C475. Writing to these registers and bits has no effect. Returns zero when read.
RO	**read only :** is used to indicate that registers and bits are read only type. Writing to these registers and bits has no effect.
R/W	**read/write :** is used to indicate that registers and bits are readable and writable.
WO	**write only :** is used to indicate that registers and bits are write only type. Writing to these registers and bits has no effect. Returns zero when read.
RC	**read clear :** is used to indicate that registers and bits are read only type. Reading these registers and all bits clear. Writing to these registers and bits has no effect.
R/WC	**read/write clear :** is used to indicate that registers and bits are readable and writable. Writing a 1 to these registers and bits clears the corresponding field. Writing a 0 to them has no effect.

5 PCI CONFIGURATION REGISTERS

5.1 Overview

The 5C475 supports PCI-CardBus Bridge Interface functions for one PC Card socket. The configuration space can be configured in compliance with the PCI Local Bus Specification Revision 2.1.

5.2 Configuration

The 5C475 supports only Type0 PCI configuration cycles(AD[1:0]=00).x The bridge configuration registers for the socket A are addressed as a function #0 with AD[10:8] as shown in the following table. Attempted access of a register in the 1-7 function range results in no response by RL5C465 and a PCI-master abort.

AD[10:8]	5C475 PCI Function Addressed
000	#0: PCI-CardBus bridge for socket A
001-111	none (Reserved)

5.3 Register Configuration

Logically the 5C475 looks to the primary PCI as two separate secondary buses residing in a single device. Each socket has its own configuration space. This makes the bridge a multi-function device. The 5C475 implements a 256 bytes configuration space. This space is divided into a predefined header space and a device dependent space. The first 64 bytes in each socket is defined the same predefined header format for all types of devices. The remaining 192 bytes is used as an unique configuration space can have different layouts depending on the base function in each socket.

The 5C475 configuration space is accessible only from the primary PCI bus. No other interfaces respond to configuration cycles. Based on the configuration command (Read/Write) and the C/BE[3:0]# lines, the 5C475 will provide data from selected register or write the data proffered. Read data will be all 32-bit DWORD register, regardless of byte enables, with the requested data driven in its natural byte location. Write data will be deposited into the selected register using the C/BE[3:0]# lines to enable the write.

The PCI configuration register is consisted of the 8-bit BYTE register, the 16-bit WORD register and the 32-bit DWORD register. During a configuration access cycle, the PCI configuration register is accessed using a 32-bit DWORD. The C/BE[3:0]# byte enable to access to specified BYTE/WORD registers.

The following tables are the 5C475 configuration registers. Some registers are not unique to a socket. These include the Vender ID, Device ID and Header Type, etc. Some bridge register are only used by some functions or one socket.

Register Space Name: PCI-CARDBUS Bridge Configuration Space

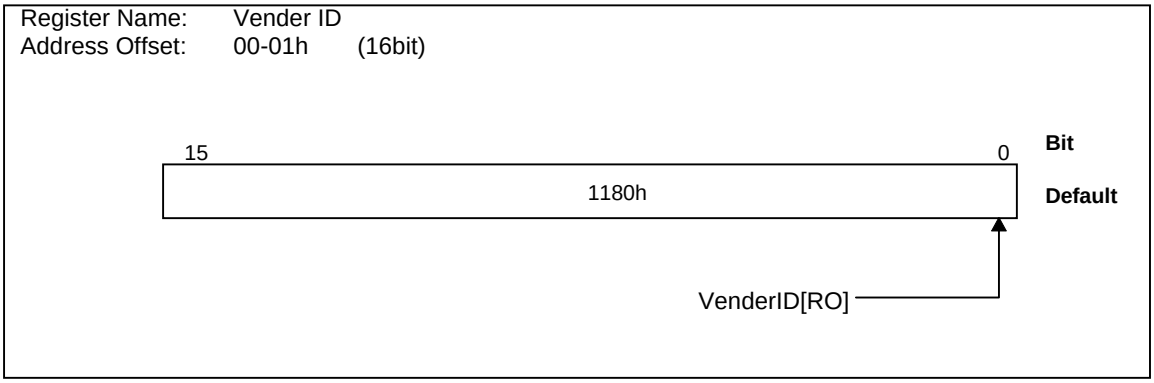
	31 24	23 16	15 8	7 0	Bit
	Device ID		Vendor ID		00h
	PCI Status		PCI Command		04h
	Class Code			Revision ID	08h
	BIST	Header Type	PCI Latency Timer	Cache Line Size	0Ch
	Card Control Registers Base Address				10h
	CardBus Status		Reserved	Cap_Ptr	14h
	CardBus Latency Timer	Subordinate Bus Number	CardBus Bus Number	PCI Bus Number	18h
	Memory Base 0				1Ch
	Memory Limit 0				20h
	Memory Base 1				24h
	Memory Limit 1				28h
	I/O Base 0 Upper		I/O Base 0 Lower		2Ch
	I/O Limit 0 Upper		I/O Limit 0 Lower		30h
	I/O Base 1 Upper		I/O Base 1 Lower		34h
	I/O Limit 1 Upper		I/O Limit 1 Lower		38h
	Bridge Control		Interrupt Pin	Interrupt Line	3Ch
	Subsystem ID		Subsystem Vender ID		40h
	16-bit Legacy Mode Base Address				44h
	Reserved				48h ~ 7Ch
	Misc Control		Bridge Configuration		80h
	Reserved		16-bit Interface Control		84h
	16-bit Memory Timing 0		16-bit I/O Timing 0		88h
	Reserved		Reserved		8Ch
	DMA Slave Configuration				90h
	Reserved				
Cap_Ptr	Power Management Capabilities		Next Item Ptr	Capability ID	DCh
Cap_Ptr+4	Data	Power Management CSR			E0h
	Reserved				

5.4 Register Description

5.4.1 Vender ID register

Register Name :	Vender ID
Address Offset :	00h-01h(16bit)
Default :	1180h
Access :	RO

This is a unique 16-bit value that is assigned to a vendor identification, and it is used with the Device ID in order to identify each PCI device. Writing to this register has no effect.

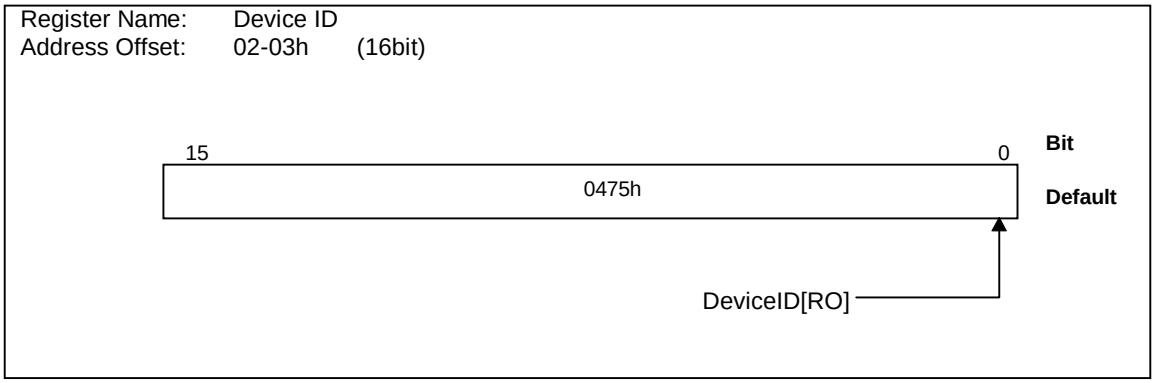


Bit	Field Name	Description
15-0	Vender ID	This read-only field is the vendor identification assigned to RICOH by the PCI Special Interest Group. This field always returns 1180h when read.

5.4.2 Device ID register

Register Name :	Device ID
Address Offset :	02h-03h(16bit)
Default :	0475h
Access :	RO

This is a unique 16-bit value that is assigned to the PCI CardBus Bridge function, and it is used with the Vendor ID in order to identify each PCI device. Writing to this register has no effect.

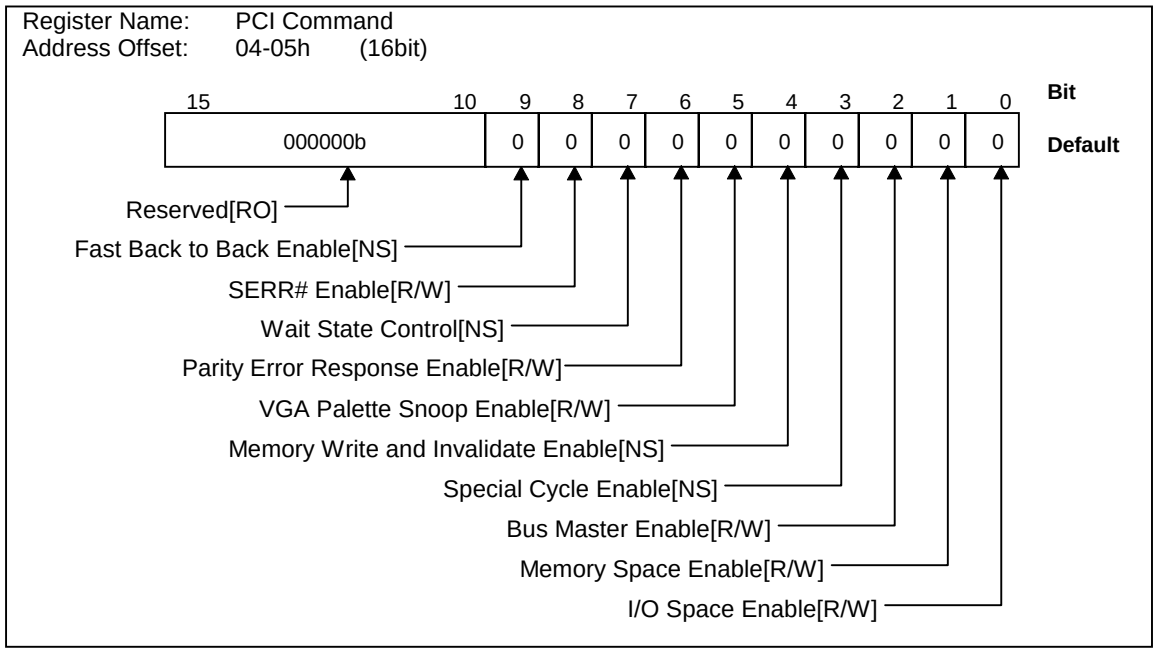


Bit	Field Name	Description
15-0	Device ID	This read-only field is the device identification assigned to the 5C475 by RICOH. This field always returns 0475h when read.

5.4.3 PCI Command register

Register Name :	PCI Command
Address Offset :	04h-05h(16bit)
Default :	0000h
Access :	R/W

The PCI Command Register controls the 5C475's responses to PCI Bus transactions on the primary interface. When this register has a value of '0', the function accepts only configuration accesses. The bits, with the exception of VGA Palette Snoop bit, in this register adhere to the definitions in the PCI Local Bus Specification.

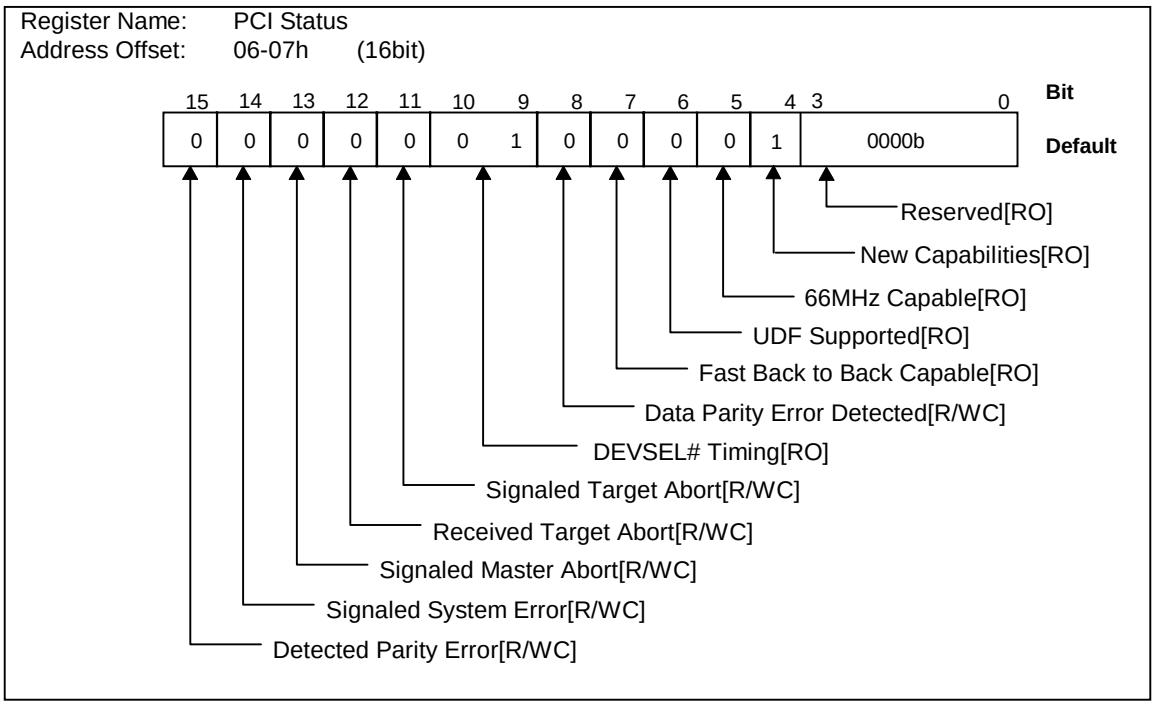


Bit	Field Name	Description
15-10	Reserved	These bits are reserved for future use by PCI Local Bus Specification Version2.1. This field always returns zero when read.
9	Fast Back to Back Enable	This bit controls whether or not the PCI master dose fast back-to-back transactions. But, this function is not implemented in the 5C475. This bit always returns zero when read. Writing to this field has no effect.
8	SERR# Enable	This bit controls whether or not the SERR# output buffer is enabled on the PCI interface. The default after reset is zero. 0 - disable the SERR# driver. 1 - enable the SERR# driver. This bit must be set to report address parity errors.
7	Wait Cycle Control	This bit controls whether or not a card does address/data stepping. But, this function is not implemented in the 5C475. This bit always returns zero when read. Writing to this field has no effect.
6	Parity Error Response Enable	This bit controls the device's response to parity errors. When this bit is set to 1, the 5C475 takes its normal action - enable an error bit and assert PERR#, when a parity error is detected. When this bit is set to 0, the 5C475 ignores any parity errors and continue normal operation. The default after reset is zero.
5	VGA Palette Snoop Enable	This bit controls the 5C475's response to VGA palette registers. When this bit is set to 1, palette snooping is enabled (AD[9:0] = 3C6h, 3C8h and 3C9h are decoded, AD[15:10] are not). The 5C475 forwards these addresses to the CardBus interface. Conversely, the 5C475 ignores to read from these addresses on the CardBus interface. When this bit is set to 0, the 5C475 ignores palette accesses. The default after reset is zero.
4	Memory Write and Invalidate Enable	This bit controls whether or not the PCI master uses the Memory Write and Invalidate command. But, this function is not implemented in the 5C475. This bit always returns zero when read. Writing to this field has no effect.
3	Special Cycle Enable	This bit controls an action on Special Cycle operations. But, this function is not implemented in the 5C475. This bit always returns zero when read. Writing to this field has no effect.
2	Bus Master Enable	This bit controls the 5C475's ability to operate as a master on the PCI interface. Setting this bit has no effect upon the configuration command operations. When this bit is set to 0, the 5C475 ignores all memory or I/O transactions on the CardBus interface. The default after reset is zero. 0 - inhibit the 5C475 to operate as a master on the PCI interface. 1 - allow the 5C475 to operate as a master on the PCI interface
1	Memory Space Enable	This bit controls the 5C475's response to memory accesses for both the memory mapped I/O ranges and the prefetchable memory ranges. The default after reset is zero. 0 - ignore all memory transactions on the PCI interface, and the 5C475 DEVSEL# logic is inhibited during the memory cycle. 1 - enable response to memory transactions on the PCI interface. And also, this bit controls accesses to the memory mapped I/O ranges that are defined in the Card Control Base Address register.
0	I/O Space Enable	This bit controls the 5C475's response to I/O accesses for transactions on the PCI interface. The default after reset is zero. 0 - ignore all I/O transactions on the PCI interface, and the 5C475. DEVSEL# logic is inhibited during the I/O cycle. 1 - enable response to I/O transactions on the PCI interface.

5.4.4 PCI Status register

Register Name :	PCI Status
Address Offset :	06h-07h(16bit)
Default :	0210h
Access :	RO,R/WC

This 16-bit register is used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written and the data in the corresponding bit location is a one. Writing a zero to this register has no effect. The bits in this register adhere to the definitions in the PCI Local Bus Specification, but only apply to the primary PCI interface.



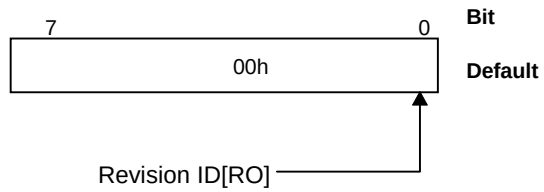
Bit	Field Name	Description
15	Detected Parity Error	This bit is set by the 5C475 whenever it detects a parity error, even if parity error handing is disabled(as controlled by bit 6 in the Command register). Writing a one to this bit clears the state.
14	Signaled System Error	This bit is set whenever the 5C475 asserts SERR#. Writing a one to this bit clears the state.
13	Signaled Master Abort	This bit is set by the 5C475 as a master device whenever its transaction is terminated with Master-abort. Writing a one to this bit clears the state.
12	Received Target Abort	This bit is set by the 5C475 as a master device whenever its transaction is terminated with Target-abort. Writing a one to this bit clears the state.
11	Signaled Target Abort	This bit is set by the 5C475 as a target device whenever its transaction is terminated with Target-abort. Writing a one to this bit clears the state.
10-9	DEVSEL# Timing	These bits encode the timing of DEVSEL#. These are encoded as 01b for medium speed. These bits are read-only. Writing to these bits has no effect.
8	Data Parity Error Detected	This bit is set when three conditions are met : 1) the bus agent asserted PERR# itself or observed PERR# asserted. 2) the agent setting the bit acted as the bus master for the operation in which the error occurred. 3) the Parity Error Response bit (Command register) is set. Writing a one to this bit has no effect.
7	Fast Back to Back Capable	This read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. The 5C475 returns zero when read, because it is not capable of accepting fast back-to-back transactions. Writing to this bit had no effect.
6	UDF Supported	This read-only bit indicates whether or not the PCI device supports the UDF function. The 5C475 doesn't support the UDF function, and therefore returns a zero when read. Writing to this bit has no effect.
5	66MHz Capable	This read-only bit indicates whether or not the PCI device is capable of running at 66MHz. The 5C475 is capable of running only at 33MHz, and therefore returns a zero when read. Writing to this bit has no effect.
4	New Capabilities	This bit indicates whether PCI device implements a list of new capabilities such as PCI Power Management. The 5C475 implements it, and therefore returns a one when read. The register at 14h provides an offset into the configuration space pointing to the location of Power Management Register Block.
3-0	Reserved	These read-only bits are reserved for future use by PCI Local Bus specification 2.1. Return a zero when read. Writing to these bits has no effect.

5.4.5 Revision ID register

Register Name :	Revision ID
Address Offset :	08h(8bit)
Default :	00h
Access :	RO

This is a unique 8-bit value that is asserted to the device revision information. It is used with the Vendor ID and the Device ID in order to identify each PCI device. Writing to this register has no effect.

Register Name: Revision ID
Address Offset: 08h (8bit)

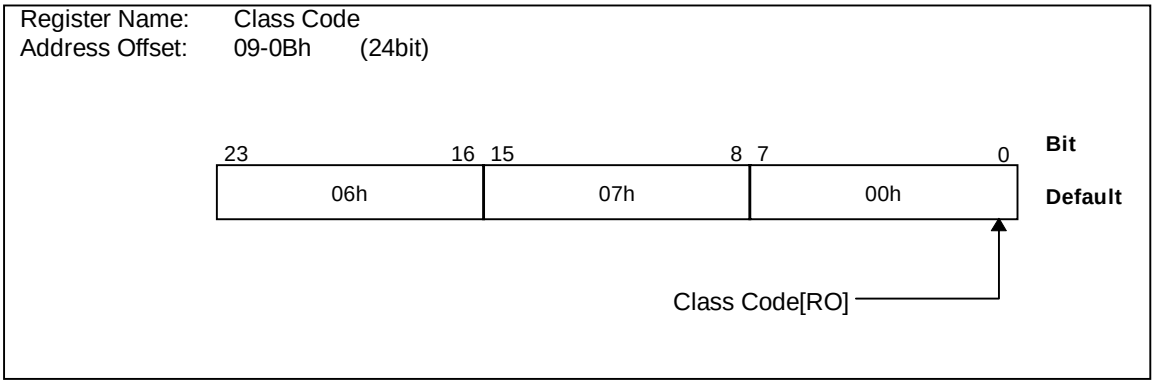


Bit	Field Name	Description
7-0	Revision ID	This read-only field is the revision identification number assigned to the 5C475 by RICOH. This field always returns zero when read.

5.4.6 Class Code register

Register Name :	Class Code
Address Offset :	09h-0Bh(24bit)
Default :	060700h
Access :	RO

The Class Code register is read-only and is used to identify the generic function of the device. The bits in this register adhere to the definitions in the PCI Local Bus Specification. This register is broken into three byte-size fields : a base class code, a sub-class code and a programming interface. Writing to this register has no effect.



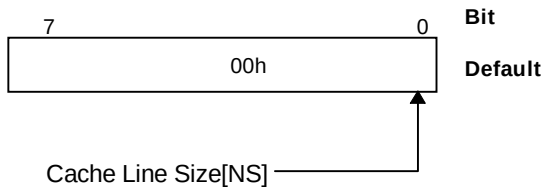
Bit	Field Name	Description
23-0	Class Code	This register is a read-only register and is used to identify the device. This register is broken into three byte-size fields. The upper byte (at offset 0Bh) is a base class code. The middle byte (at offset 0Ah) is a sub-class coded. The lower byte (at offset 09h) identifies a specific register-level programming interface. The 5C475 returns 060700h when this register is indicated as a PCI-CardBus bridge device : a base class of 06h (bridge device), a sub-class code of 07h (PCI to CardBus) and a programming interface of 00h. Writing to this register has no effect.

5.4.7 Cache Line Size register

Register Name :	Cache Line Size
Address Offset :	0Ch(8bit)
Default :	00h
Access :	NS

The Cache Line register specifies the system cache line size in units of 32-bit words. The 5C475 doesn't participate in the caching protocol, and therefore returns zero when read. Writing to this register has no effect.

Register Name: Cache Line Size
Address Offset: 0Ch (8bit)



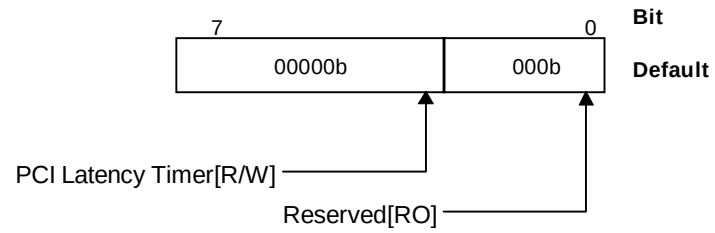
Bit	Field Name	Description
7-0	Cache Line Size	The 5C475 doesn't participate in the caching protocol. This register is read-only. Returns zero when read. Writing to this register has no effect.

5.4.8 PCI Latency Timer register

Register Name :	PCI Latency Timer
Address Offset :	0Dh(8bit)
Default :	00h
Access :	R/W

The PCI Latency Timer specifies, in units of PCI bus clocks, the value of the Latency Timer for the PCI bus master. This register adheres to the PCI Local Bus Specification but applies only to the primary interface. The bottom three bits in this register are read-only and hardwired to 000b, resulting in a timer granularity of eight clocks.

Register Name: PCI Latency Timer
Address Offset: 0Dh (8bit)

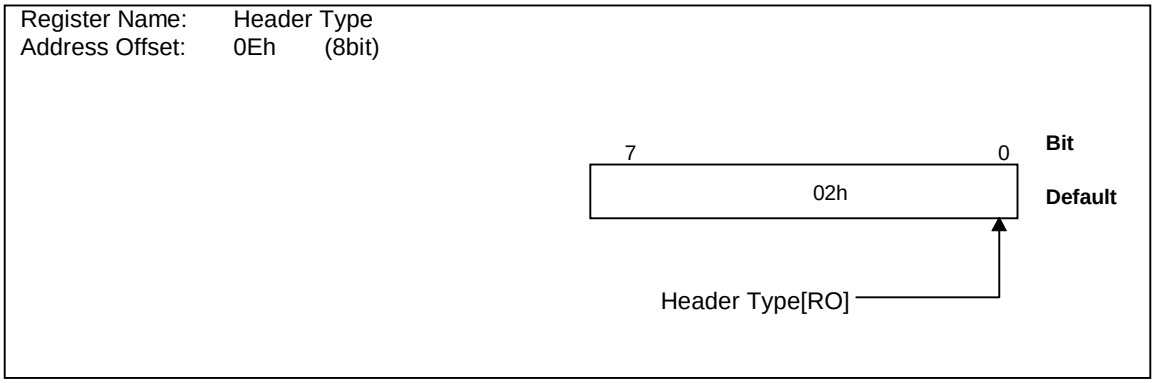


Bit	Field Name	Description
7-3	PCI Latency Timer	This register specifies, in units of PCI bus clocks, the value of the Latency Timer for the PCI bus master.
2-0	Reserved	The bottom three bits in this register are read-only and hardwired to 000b, resulting in a timer granularity of eight clocks. Writing to this field has no effect.

5.4.9 Header Type register

Register Name :	Header Type
Address Offset :	0Eh(8bit)
Default :	02h
Access :	RO

The Header Type register identifies the layout of bytes 10h through 3Fh in configuration space and also whether or not the device contains multiple function. The 5C475 is the multi-function device and the PCI-CardBus bridge, and therefore returns 02h when read. Writing to this register has no effect.



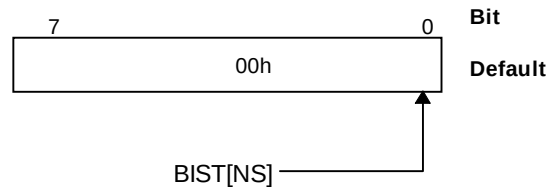
Bit	Field Name	Description
7-0	Header Type	This register identifies the layout of bytes 10h through 3Fh in configuration space and also whether or not the device contains multiple functions. Return 02h when read. Writing to this register has no effect.

5.4.10 BIST register

Register Name :	BIST
Address Offset :	0Fh(8bit)
Default :	00h
Access :	NS

The BIST register is used for control and status of BIST(Built In Self Test). The bits in this register adhere to the definitions in the PCI Local Bus Specification. The 5C475 does not implement BIST, and therefore returns zero when read.

Register Name: BIST
Address Offset: 0Fh (8bit)



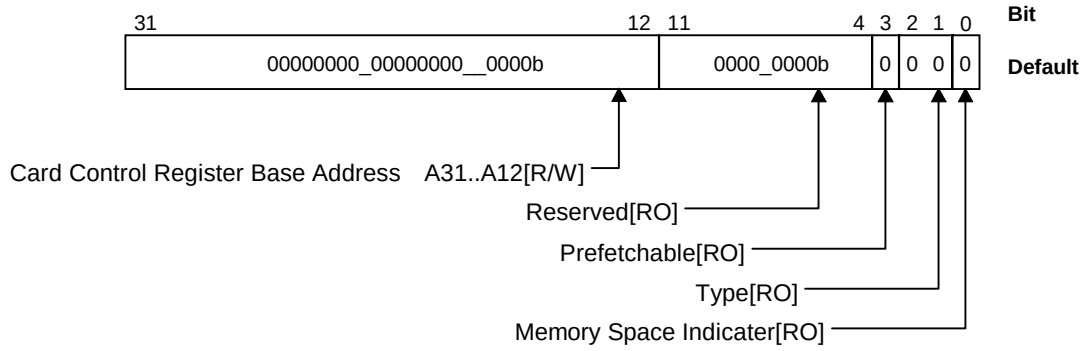
Bit	Field Name	Description
7-0	BIST	The 5C475 doesn't support this register. This read-only register always returns zero when read. Writing to this register has no effect.

5.4.11 Card Control Register Base Address register

Register Name :	Card Control Register Base Address
Address Offset :	10h(32bit)
Default :	0000_0000h
Access :	R/W

The Card Control Register Base Address register points to the memory mapped I/O space that contains Status and Control registers for both the PC Card-32 and the PC Card-16. The upper bits [31:12] are read/write and the lower bits [11:0] are hardwired to zero. This indicates to Configuration software that the 5C475 must take 4K bytes of non-prefetchable memory space. The PC Card-32 (CardBus Card) Status and Control registers start at offset 000h (in the bottom 2K bytes) and the PC Card-16 registers start at offset 800h (in the top 2K bytes). The 5C475 dose not respond to PCI cycles unless specifically loaded with a non-zero address after PCIRST# is deasserted.

Register Name: Card Control Register Base Address
Address Offset: 10h (32bit)

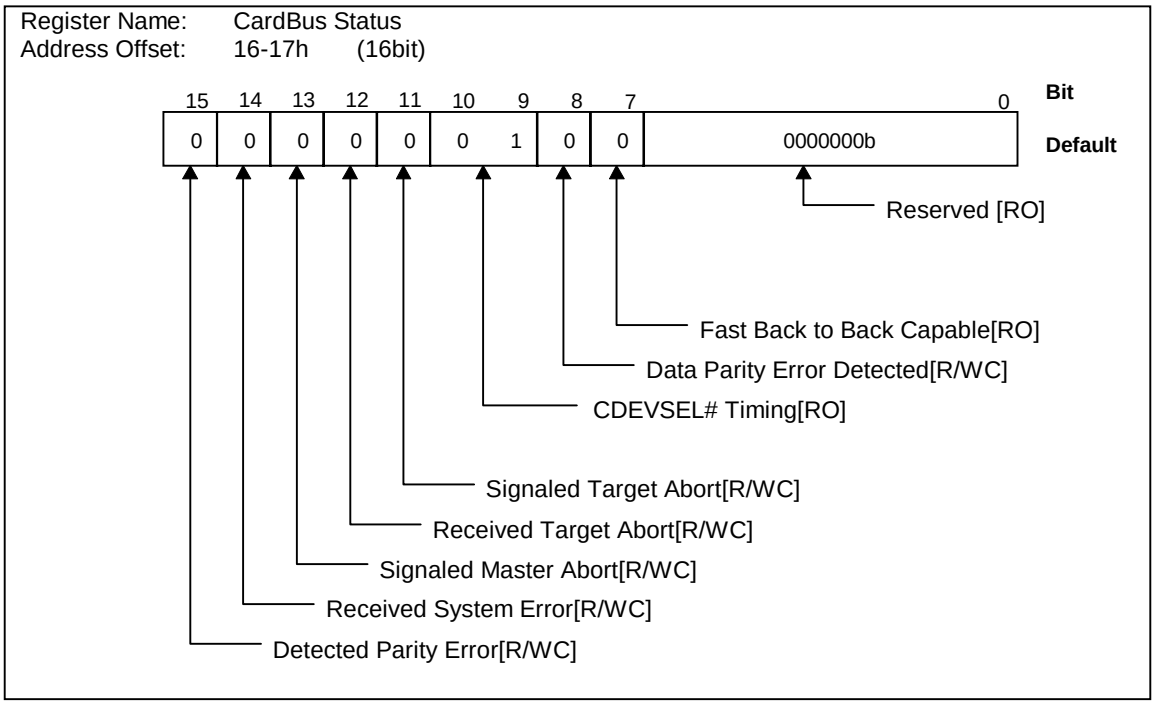


Bit	Field Name	Description
31-12	Card Control Register Base Address A31..A12	These bits indicate the memory mapped I/O space that contains status and control registers for both the PC Card-32 and the PC Card-16. Bits [31:12] are read/write.
11-4	Reserved	These bits are read-only and hardwired to zero. Writing to this field has no effect.
3	Prefetchable	This bit is set to one when the data is prefetchable and reset to a zero otherwise. This filed is hardwired to zero in the 5C475. Writing to this field has no effect.
2-1	Type	These bits have encoded meanings as shown below for Memory Base Address registers. 00 : locate anywhere in 32-bit address space 01 : locate below 1M 10 : locate anywhere in 64-bit address space 11 : reserved This field is read-only and hardwired to zero in the 5C475. Writing to this field has no effect.
0	Memory Space Indicator	This bit indicates the Base Address register maps into either a memory space or an I/O space. This field returns zero when the register maps into a memory space and one when the register maps into a I/O space. This field is read-only and hardwired to zero in the 5C475. Writing to this field has no effect.

5.4.12 CardBus Status register

Register Name :	CardBus Status
Address Offset :	16h-17h(16bit)
Default :	0200h
Access :	RO,R/WC

The CardBus Status register is used to record status information for CardBus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written and the data in the corresponding bit location is a one. Writing a zero to this register has no effect. The bits in this register adhere to the definitions in the PCI Local Bus Specification, but only apply to the secondary CardBus interface.

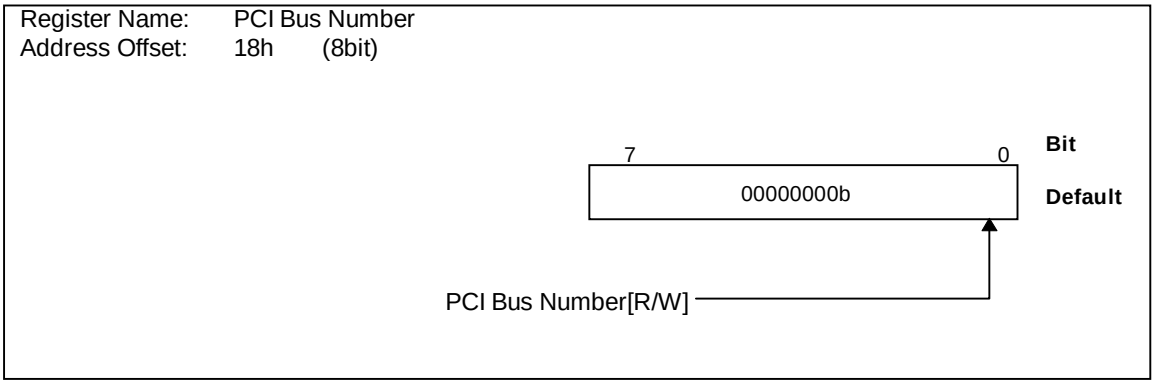


Bit	Field Name	Description
15	Detected Parity Error	This bit is set by the 5C475 whenever it detects a parity error on the secondary bus, even if parity error handing is disabled (as controlled by bit 6 in the Command register). Writing a one to this bit clears the state.
14	Received System Error	This bit is set whenever the 5C475 receives CSERR#. Writing a one to this bit clears the state. When both CSERR# enable bit in the Bridge Control register and SERR# enable bit in the PCI Command register are set, the 5C475 asserts SERR# on the primary PCI bus whenever it receives CSEER#.
13	Signaled Master Abort	This bit is set by the 5C475 as a master device on the CardBus interface whenever its transaction is terminated with master-abort. Writing a one to this bit clears the state.
12	Received Target Abort	This bit is set by the 5C475 as a master device on the CardBus interface whenever its transaction is terminated with target-abort. Writing a one to this bit clears the state.
11	Signaled Target Abort	This bit is set by the 5C475 as a target device on the CardBus interface whenever its transaction is terminated with target-abort. Writing a one to this bit clears the state.
10-9	CDEVSEL# Timing	This field encodes the timing of CDEVSEL#. These read-only bits are encoded as 01b for medium speed in the 5C475. Writing to this field has no effect.
8	Data Parity Error Detected	This bit is set by a CardBus master when three conditions are met : 1) the bus agent asserted CPERR# itself or observed CPERR# asserted. 2) the agent setting the bit acted as the bus master for the operation in which the error occurred. 3) the Parity Error Response bit (Control register) is set. Writing a one to this bit clears the state.
7	Fast Back to Back Capable	This read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not the same agent. The 5C475 returns a zero when read, because it is not capable of fast back-to-back transactions on the CardBus interface. Writing to this bit has no effect.
6-0	Reserved	This bit is reserved for future use by the PCI Local Bus specification 2.1. This field is read-only. Returns zero when read. Writing to this field has no effect.

5.4.13 PCI Bus Number register

Register Name :	PCI Bus Number
Address Offset :	18h(8bit)
Default :	00h
Access :	R/W

The PCI Bus Number register indicates the number of the PCI bus on the primary side of the 5C475. This is set by the appropriate configuration software. The 5C475 doesn't decode Type 1 configuration transactions on the CardBus interface that should be converted to Special Cycle transactions on PCI bus interface.

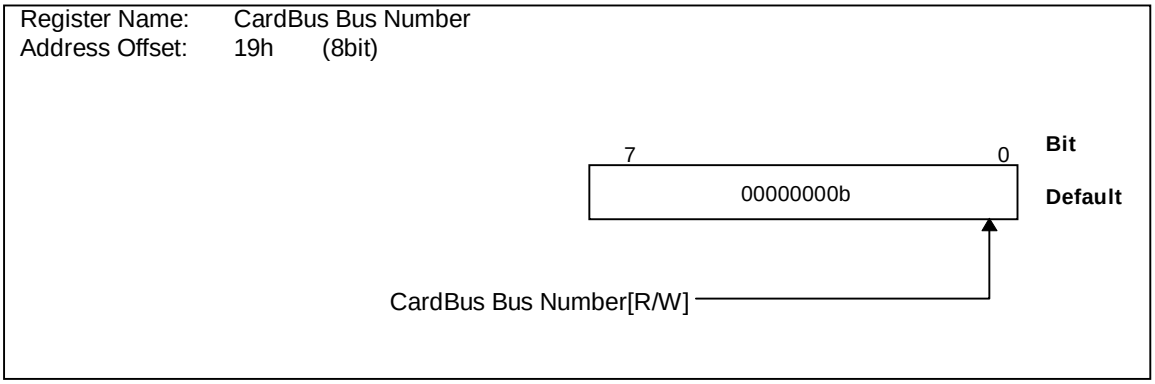


Bit	Field Name	Description
7-0	PCI Bus Number	This field indicates the number of the PCI bus on the primary side of the 5C475. This field is read/write, but this register has no effect upon the 5C475's operation. The default after reset is zero.

5.4.14 CardBus Bus Number register

Register Name :	CardBus Bus Number
Address Offset :	19h(8bit)
Default :	00h
Access :	R/W

The CardBus Bus Number register indicates the number of the CardBus attached to the socket. This register that is read/write is set by the appropriate configuration software or the socket services software. The 5C475 uses this register to convert Type 1 configuration transactions on the primary (PCI) interface to Type 0 transactions on the secondary (CardBus) interface.

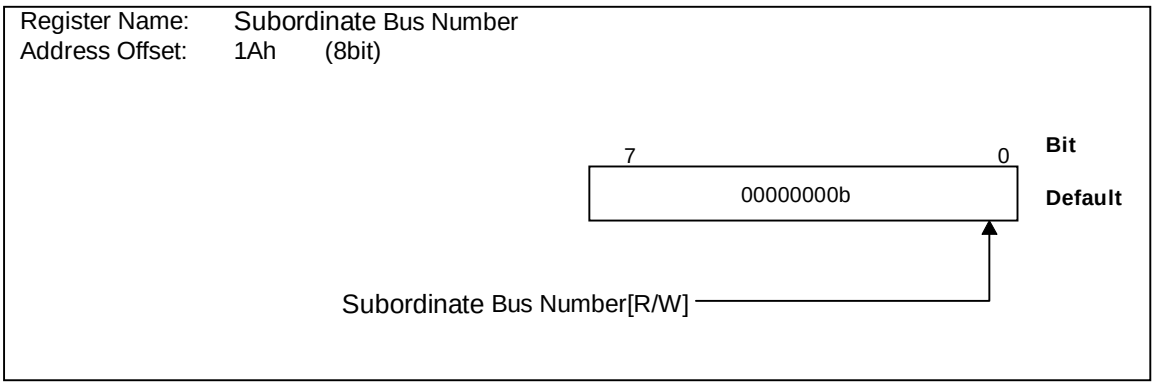


Bit	Field Name	Description
7-0	CardBus Bus Number	This register indicates the number of the CardBus attached to the socket. This is set by the appropriate configuration software or the socket services software. If the values of a Bus Number field agree with the values of this register on a Type 1 configuration transactions on the primary (PCI) interface, the 5C475 converts them to a Type 0 configuration transactions on the secondary (CardBus) interface. The default after reset is zero.

5.4.15 Subordinate Bus Number register

Register Name :	Subordinate Bus Number
Address Offset :	1Ah(8bit)
Default :	00h
Access :	R/W

The Subordinate Bus Number register is used to record the number of the bus at the lowest part of the hierarchy behind the bridge. This register that is read/write is set by the appropriate configuration software or the socket services software. Normally, a CardBus bridge will be at the bottom of the bus hierarchy and this register will hold the same value as the CardBus Bus Number register. The 5C475 uses this register in conjunction with the Card Bus Number register to convert Type 1 configuration transactions on the primary (PCI) interface to Type 0 or 1 configuration transactions on the secondary interface.



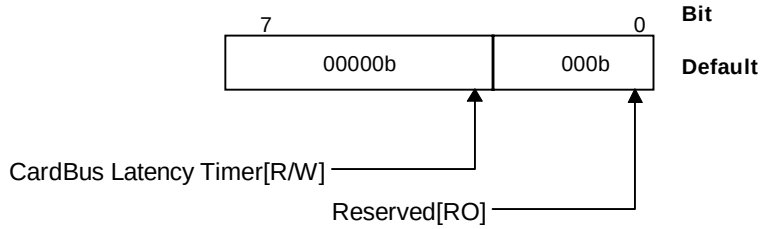
Bit	Field Name	Description
7-0	Subordinate Bus Number	This register is used to record the number of the bus at the lowest part of the hierarchy behind the 5C475. This register that is read/write is set by the appropriate configuration software or the socket services software. Normally, a CardBus bridge will be at the bottom of the bus hierarchy and this register will hold the same value as the CardBus Bus Number register. When the value of Bus Number field is more over the CardBus Bus Number register's and less than this register's in Type 1 configuration cycles on the primary (PCI) interface, the 5C475 converts the value to Type1 configuration cycles on the secondary (CardBus) interface. The default after reset is zero.

5.4.16 CardBus Latency Timer register

Register Name :	CardBus Latency Timer
Address Offset :	1Bh(8bit)
Default :	00h
Access :	R/W

The CardBus Latency Timer register has the same functionality of the primary PCI bus Latency Timer but applies to the CardBus attached to this specific socket. This is set by the PCI BIOS configuration software or the socket services software. This register adheres to the PCI Local Bus Specification but applies only to the primary interface. The bottom three bits in this register are read-only and hardwired to zeros, resulting in a timer granularity of eight clocks.

Register Name: CardBus Latency Timer
Address Offset: 1Bh (8bit)

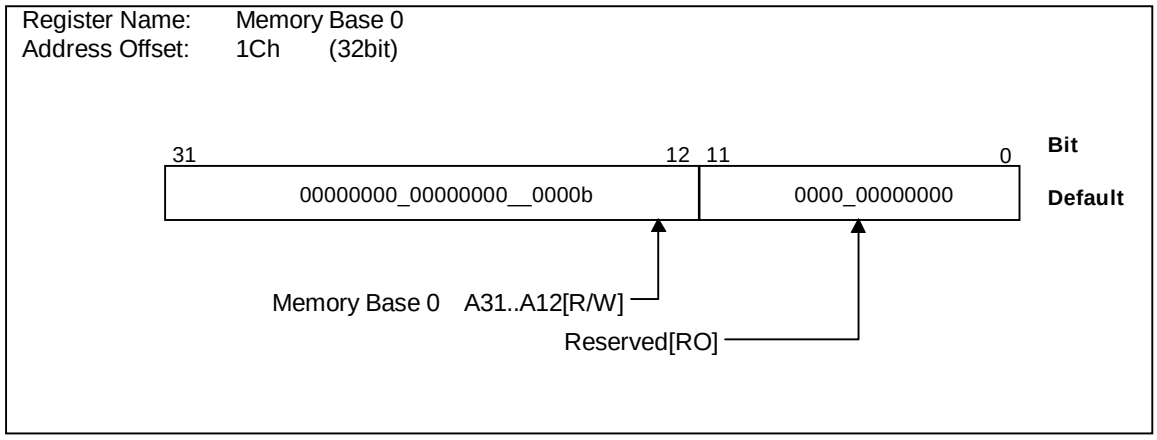


Bit	Field Name	Description
7-3	CardBus Latency Timer	This field specifies, in units of CardBus clocks, the value of the Latency Timer for the CardBus master.
2-0	Reserved	These bits are read-only and hardwired to 000b, resulting in a timer granularity of eight clocks. Writing to this field has no effect.

5.4.17 Memory Base 0 register

Register Name :	Memory Base 0
Address Offset :	1Ch(32bit)
Default :	0000_0000h
Access :	R/W

The Memory Base #0 register indicates the bottom address of a memory mapped I/O window #0. The upper 20-bits correspond to address bits AD[31:12] that is read/write. The bottom 12-bits of this register are read-only and hardwired to zeros. This window is enabled by the Memory Space Enable bit (bit1) in the Command register. The Memory #0 Prefetch Enable bit (bit8) in the Bridge Control register specifies whether the memory window is prefetchable or non-prefetchable. The default of this bit is prefetchable, but this bit must be non-prefetchable only when side effects are caused by memory read command on the installed CardBus card. This register has no meaning for PC Card-16.

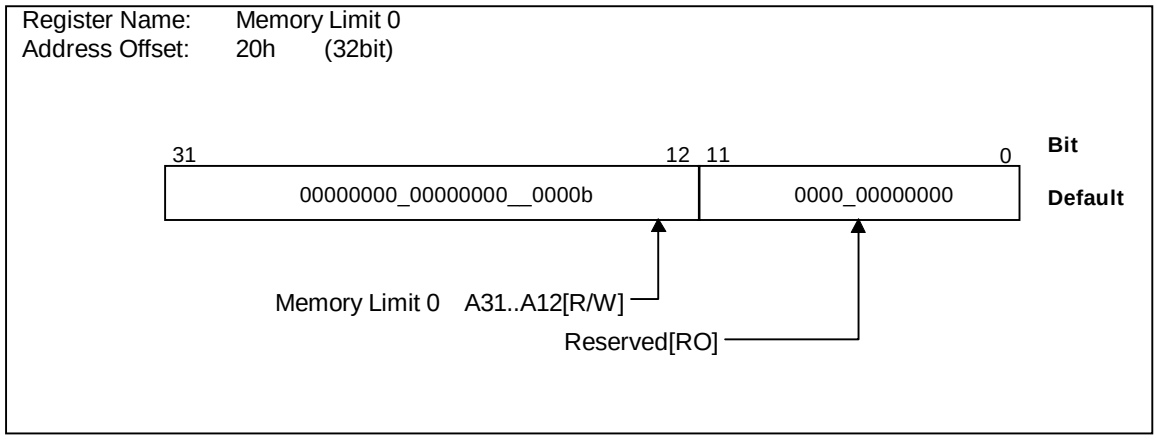


Bit	Field Name	Description
31-12	Memory Base 0 A31..A12	This register indicates the base address of a memory mapped I/O range that are used by the RL5C476/478 to determine when to forward memory transactions from PCI interface to CardBus interface. This field is read/write.
11-0	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect.

5.4.18 Memory Limit 0 register

Register Name :	Memory Limit 0
Address Offset :	20h(32bit)
Default :	0000_0000h
Access :	R/W

The Memory Limit #0 register indicates the top address of the memory mapped I/O space #0. The upper 20-bits correspond to address bits AD[31:12] that are read/write. The bottom 12-bits of this register are read-only and hardwired to zeros. The bridge assumes the bottom address bits [11:0] are ones when the address range is decoded. So if the Memory Base and Limit registers are set to the same value, a window of 4Kbyte is defined. Both Memory windows #0 and #1 are enabled by the Memory Space Enable bit in the PCI Command register. To disable either window individually, the Limit register of that range should be set below the Base register. This will cause the bridge to never detect a hit on that window. This register has no meaning for PC Card-16.

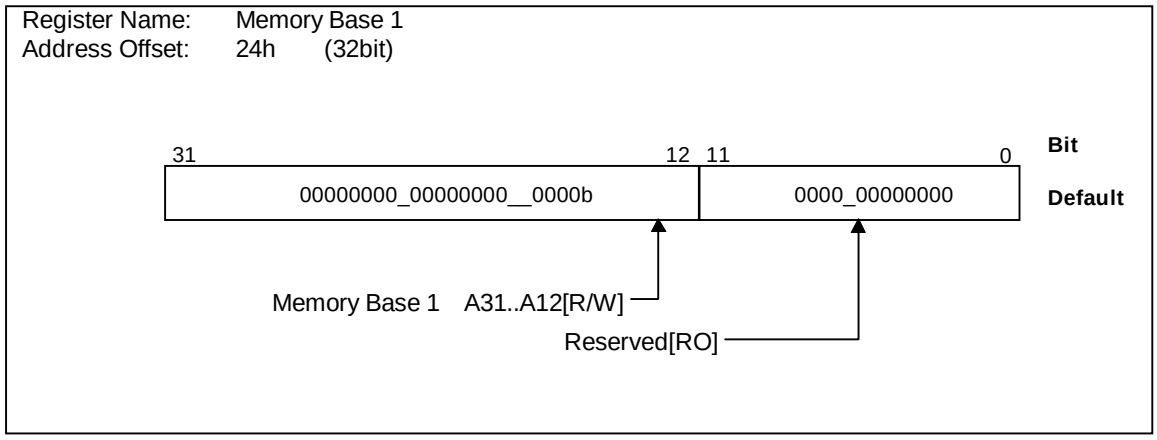


Bit	Field Name	Description
31-12	Memory Limit 0 A31..A12	This field indicates the top address of a PCI memory address range that is used by the 5C475 to determine when to forward memory transactions from the PCI interface to the CardBus interface.
11-0	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect.

5.4.19 Memory Base 1 register

Register Name :	Memory Base 1
Address Offset :	24h(32bit)
Default :	0000_0000h
Access :	R/W

The Memory Base #1 register indicates the bottom address of a memory mapped I/O window #1. The top 20-bits correspond to address bits AD[31:12] that are read/write. The bottom 12-bits of this register are read-only and hardwired to zeros. This window is enabled by the Memory Space Enable bit (bit1) in the Command register. The Memory #1 Prefetch Enable bit (bit8) in the Bridge Control register specifies whether the memory window is prefetchable or non-prefetchable. The default of this bit is prefetchable, but this bit must be non-prefetchable only when side effects are caused by memory read command on the installed CardBus card. This register has no meaning for PC Card-16.

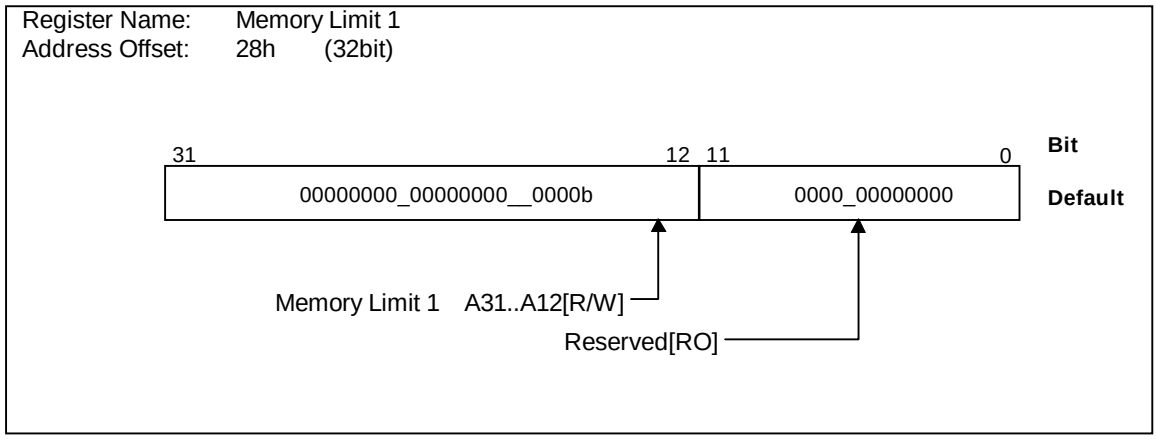


Bit	Field Name	Description
31-12	Memory Base 1 A31..A12	This field indicates the base address of a memory mapped I/O range that is used by the 5C475 to determine when to forward memory transactions from the PCI interface to the CardBus interface.
11-0	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect.

5.4.20 Memory Limit 1 register

Register Name :	Memory Limit 1
Address Offset :	28h(32bit)
Default :	0000_0000h
Access :	R/W

The Memory Limit #1 register indicates the top address of a memory mapped I/O window #1. The upper 20-bits correspond to address bits AD[31:12] that are read/write. The bottom 12-bits of this register are read-only and hardwired to zeros. The bridge assumes the bottom address bits [11:0] are ones when the address range is decoded. So if the Memory Base and Limit registers are set to the same value, a window of 4Kbyte is defined. Both Memory windows #0 and #1 are enabled by the Memory Space Enable bit in the PCI Command register. The address range of the Limit register must be set below the Base in order to disable only the Memory window #1. This register has no meaning for PC Card-16.

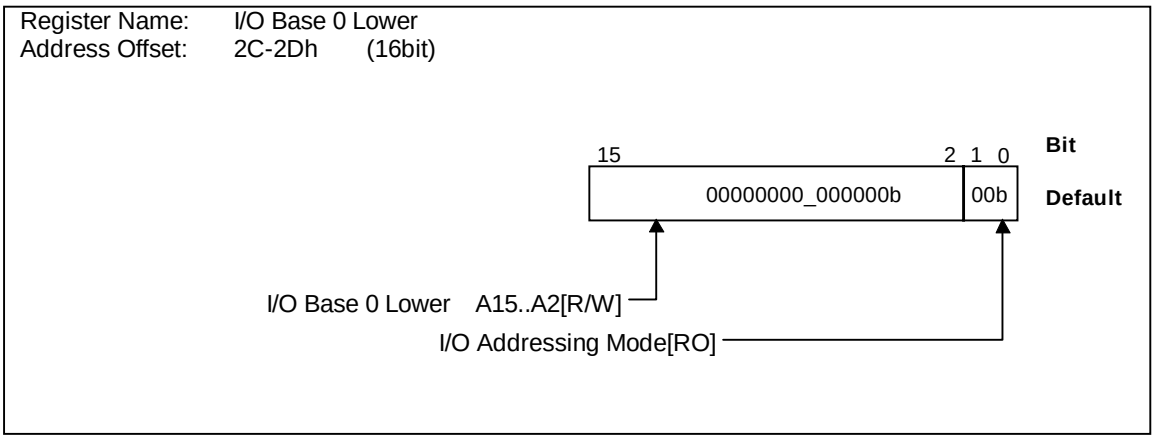


Bit	Field Name	Description
31-12	Memory Limit 1 A31..A12	This field indicates the top address of a PCI memory address range that is used by the 5C475 to determine when to forward memory transactions from the PCI interface to the CardBus interface.
11-0	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect.

5.4.21 I/O Base 0 Lower register

Register Name :	I/O Base 0 Lower
Address Offset :	2C-2Dh(16bit)
Default :	0000h
Access :	R/W

The I/O Base #0 Lower register indicates the bottom address of a PCI I/O address range that used by the 5C475 to determine when to forward an I/O transaction to the CardBus. The bits in this register correspond to AD[15:2] that are read/write, and the read-only bits AD[1:0] are used to indicate whether the bridge implements 16 or 32 bits I/O addressing. If these bits have the value 0, then the bridge implements only 16-bit I/O addressing and assumes that the upper 16 address bits AD[31:16] of the I/O base address register are zero. And if they have the value 1, then the bridge implements 32-bit I/O addressing and the 16 bits of the base register hold the upper 16 bits corresponding to AD[31:16] of the 32-bit I/O address space. This I/O window #0 is enabled by the I/O Space Enable bit in the PCI Command register. This register has no meaning for PC Card-16.

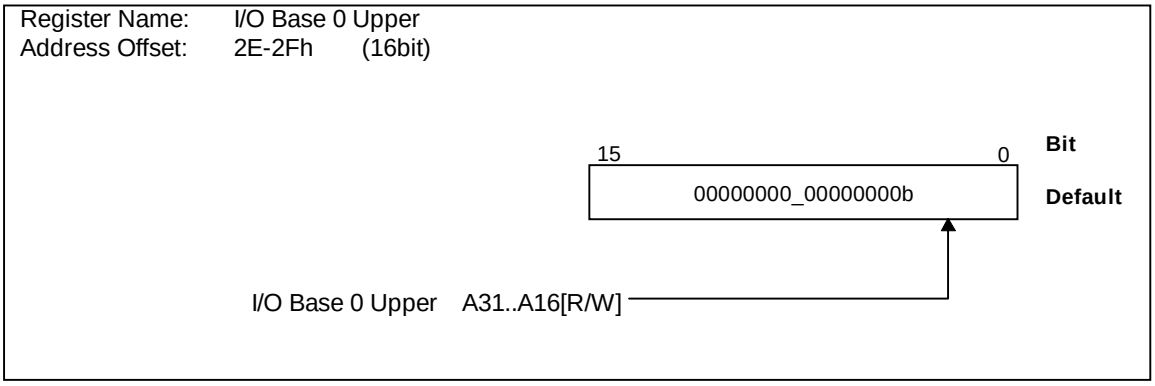


Bit	Field Name	Description
15-2	I/O Base 0 Lower A15..A2	This field indicates the base address of an address range that is used by the 5C475 to determine when to forward an I/O transaction from PCI interface to the CardBus interface.
1-0	I/O Addressing Mode	This field is read-only and returns 00b on the 16-bit I/O addressing mode, and returns on 01b on the 32-bit addressing mode. Writing to this field has no effect.

5.4.22 I/O Base 0 Upper register

Register Name :	I/O Base 0 Upper
Address Offset :	2E-2Fh(16bit)
Default :	0000h
Access :	R/W

The I/O Base #0 Upper register indicates the bottom address of an address range that is used by the 5C475 to determine when to forward an I/O transaction to the CardBus. The bits in this register correspond to AD[31:16]. Setting to this register is enabled only when the 5C475 is set on the 32-bit I/O addressing mode. This register has no meaning for PC Card-16.

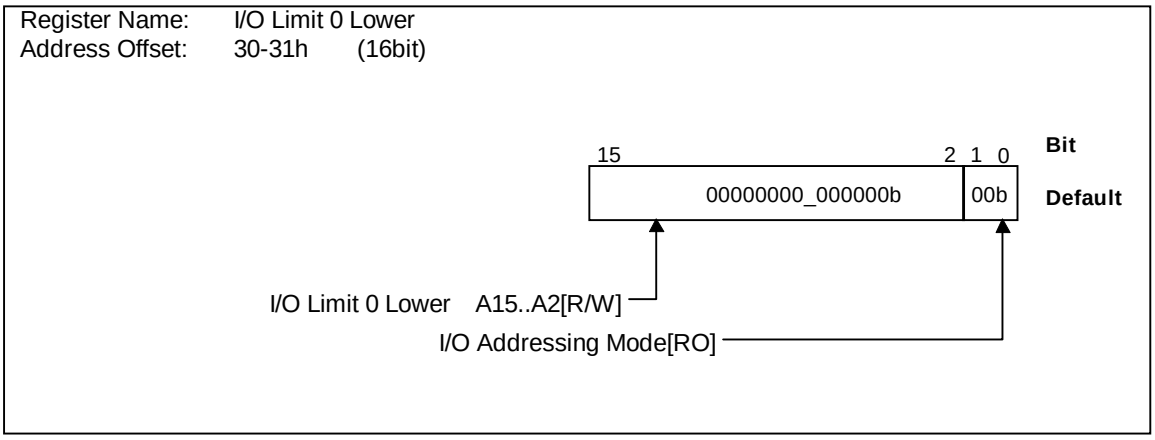


Bit	Field Name	Description
15-0	I/O Base 0 Upper A31..A16	This field indicates the base address of an address range that is used by the 5C475 to determine when to forward an I/O transaction from the PCI interface to the CardBus interface. The bits in this register correspond to AD[31:16].

5.4.23 I/O Limit 0 Lower register

Register Name :	I/O Limit 0 Lower
Address Offset :	30-31h(16bit)
Default :	0000h
Access :	R/W

The I/O Limit #0 Lower register indicates the top address of an address range that is used by the 5C475 to determine when to forward an I/O transaction to the CardBus. The bits in this register correspond to AD[15:2] that are read/write, and the read-only bits AD[1:0] are used to indicate whether the bridge implements 16 or 32 bits I/O addressing. Both I/O windows #0 and #1 are enabled by the I/O Space Enable bit in the PCI command register. This register has no meaning for PC Card-16.

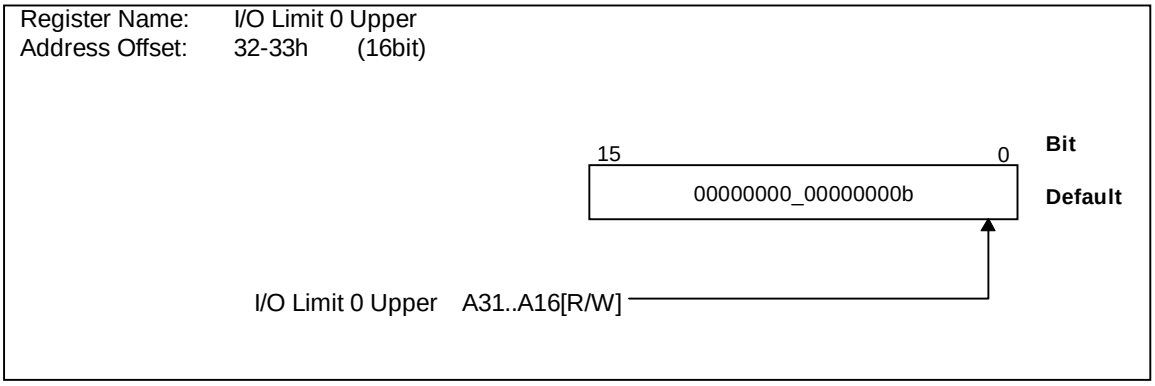


Bit	Field Name	Description
15-2	I/O Limit 0 Lower A15..A2	This field indicates the limit address of an address range that is used by the 5C475 to determine when to forward an I/O transaction from the PCI interface to the CardBus interface.
1-0	I/O Addressing Mode	This field is read-only and returns 00b on the 16-bit I/O addressing mode, and returns 01b on the 32-bit I/O addressing mode. Writing to this field has no effect.

5.4.24 I/O Limit 0 Upper register

Register Name :	I/O Limit 0 Upper
Address Offset :	32-33h(16bit)
Default :	0000h
Access :	R/W

The I/O Limit #0 Upper register indicates the limit address of an address range that is used by the 5C475 to determine when to forward an I/O transaction to the CardBus. The bits in this register correspond to AD[31:16]. Setting to this register is enabled only when the 5C475 is set on the 32-bit I/O addressing mode. This register has no meaning for PC Card-16.



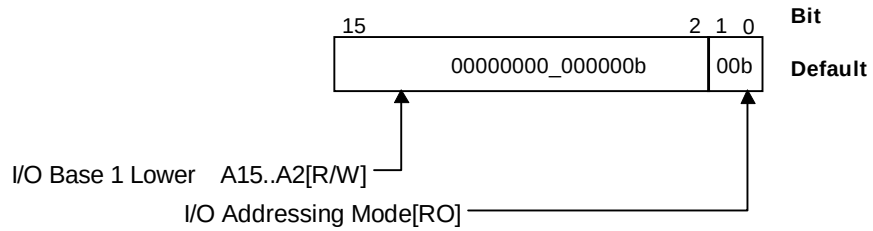
Bit	Field Name	Description
15-0	I/O Limit 0 Upper A31..A16	This field indicates the limit address of an address range that is used by the 5C475 to determine when to forward an I/O transaction to the CardBus. The bits in this register correspond to AD[31:16].

5.4.25 I/O Base 1 Lower register

Register Name :	I/O Base 1 Lower
Address Offset :	34-35h(16bit)
Default :	0000h
Address :	R/W

The I/O Base #1 register indicates the bottom address of an address range that is used by the 5C475 to determine when to forward an I/O transaction to the CardBus. The bits in this register correspond to AD[15:0]. The upper bits AD[15:2] are read/write, and the read-only bits AD[1:0] are used to indicate whether the bridge implements 16 or 32 bit I/O addressing. The I/O window #1 is enabled by the I/O Space Enable bit in the PCI Command register. This register has no meaning for PC Card-16.

Register Name: I/O Base 1 Lower
Address Offset: 34-35h (16bit)

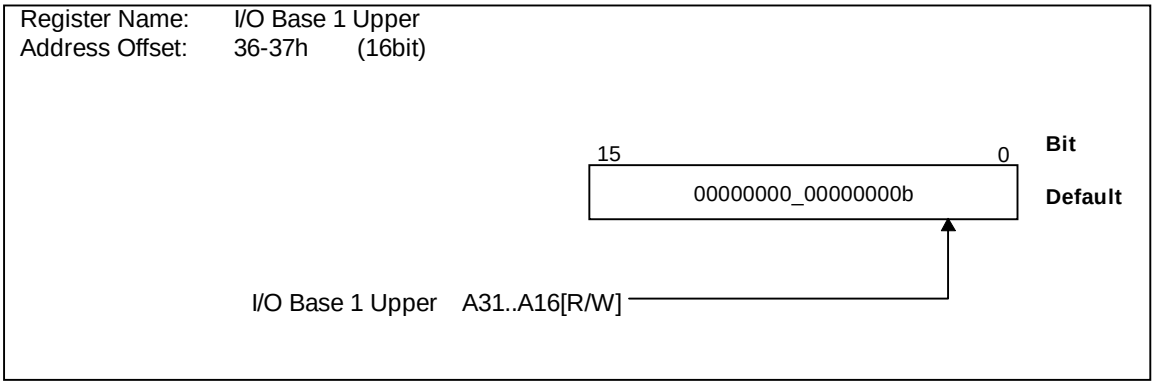


Bit	Field Name	Description
15-2	I/O Base 1 Lower A15..A2	This field indicates the base address of an address range that is used by the 5C475 to determine when to forward an I/O transaction from the PCI interface to the CardBus interface.
1-0	I/O Addressing Mode	This field is read-only and returns 00b on the 16-bit I/O addressing mode, and returns 01b on the 32-bit I/O addressing mode. Writing to this field has no effect.

5.4.26 I/O Base 1 Upper register

Register Name :	I/O Base 1 Upper
Address Offset :	36-37h(16bit)
Default :	0000h
Access :	R/W

The I/O Base #1 register indicates the bottom address of an address range that is used by the 5C475 to determine when to forward an I/O transaction to the CardBus. The bits in this register correspond to AD[31:16]. Setting to this register is enabled only when the 5C475 is set on the 32-bit I/O addressing mode. This register has no meaning for PC Card-16.



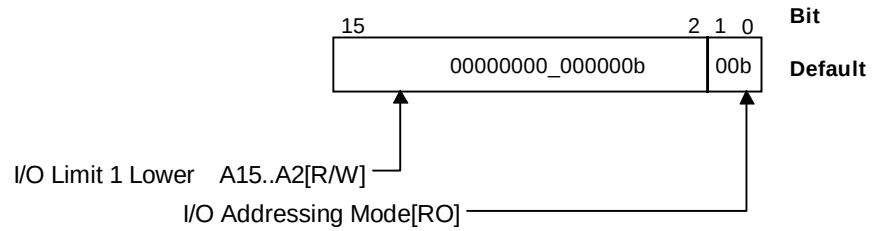
Bit	Field Name	Description
15-0	I/O Base 1 Upper A31..A16	This field indicates the base address of an address range that is used by the 5C475 to determine when to forward an I/O transaction from the PCI interface to the CardBus interface. The bits in this register correspond to AD[31:16].

5.4.27 I/O Limit 1 Lower register

Register Name :	I/O Limit 1 Lower
Address Offset :	38-39h(16bit)
Default :	0000h
Access :	R/W

The I/O Limit #1 Lower register indicates the top address of an address range that is used by the 5C475 to determine when to forward an I/O transaction to the CardBus. The bits in this register correspond to AD[15:0]. The upper bits AD[15:2] are read/write, and the read-only bits AD[1:0] are used to indicate whether the bridge implements 16 or 32 bit I/O addressing (AD[1:0] = 00b on the 16-bit I/O addressing, AD[1:0] = 01b on the 32-bit I/O addressing). Both I/O windows #0 and #1 are enabled by the I/O Space Enable bit in the PCI Command register. This register has no meaning for PC Card-16.

Register Name: I/O Limit 1 Lower
Address Offset: 38-39h (16bit)

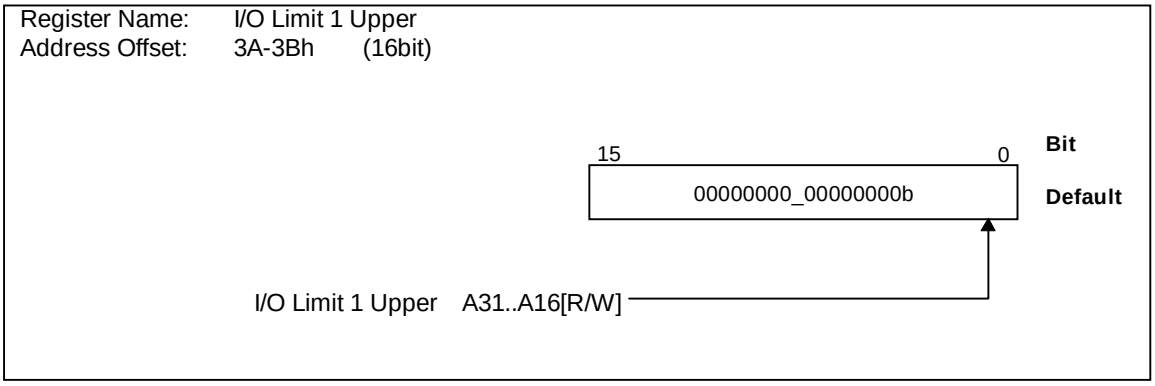


Bit	Field Name	Description
15-2	I/O Limit 1 Lower A15..A2	This field indicates the limit address of an address range that is used by the 5C475 to determine when to forward an I/O transaction from the PCI interface to the CardBus interface.
1-0	I/O Addressing Mode	This field is read-only and returns 00b on the16-bit I/O addressing mode, and returns 01b on the 32-bit I/O addressing mode. Writing to this field has no effect.

5.4.28 I/O Limit 1 Upper register

Register Name :	I/O Limit 1 Upper
Address offset :	3A-3Bh(16bit)
Default :	0000h
Access :	R/W

The I/O Limit #1 Upper register indicates the limit address of an address range that is used by the 5C475 to determine when to forward an I/O transaction to the CardBus. The bits in this register correspond to AD[31:16]. Setting to this register is enabled only when the 5C475 is set on the 32-bit I/O addressing mode. This register has no meaning for PC Card-16.

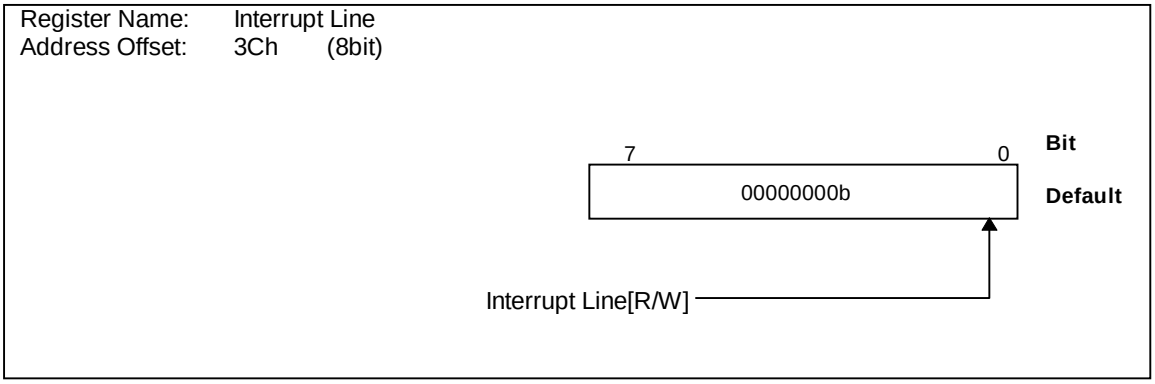


Bit	Field Name	Description
15-0	I/O Limit 1 Upper A31..A16	This field indicates the limit address of an address range that is used by the 5C475 to determine when to forward an I/O transaction to the CardBus. The bits in this register correspond to AD[31:16].

5.4.29 Interrupt Line register

Register Name:	Interrupt Line
Address Offset :	3Ch(8bit)
Default :	00h
Access :	R/W

The Interrupt Line register is read/write register used to communicate interrupt line routing information. This register must be initialized by BIOS software on the system configuration, so a default state is no specified. The value in this register indicates which input of the system interrupt controller the interrupt pin in the 5C475 is connected to. The default after reset is 00b.

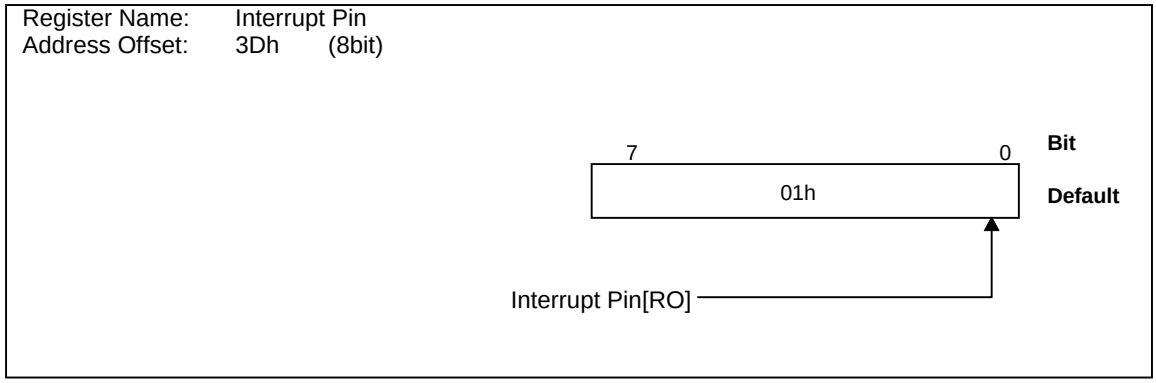


Bit	Field Name	Description
7-0	Interrupt Line	The value in this register indicates which input of the system interrupt controller the interrupt pin in the 5C475 is connected to. The default after reset is 00b.

5.4.30 Interrupt Pin register

Register Name :	Interrupt Pin
Address Offset :	3Dh(8bit)
Default :	01h
Access :	RO

The Interrupt Pin register is read-only register that adheres to the definition in the PCI Local Bus Specification. This register indicates which interrupt pin the 5C475 use. A value of 01h corresponding to INTA# is assigned to socket A.

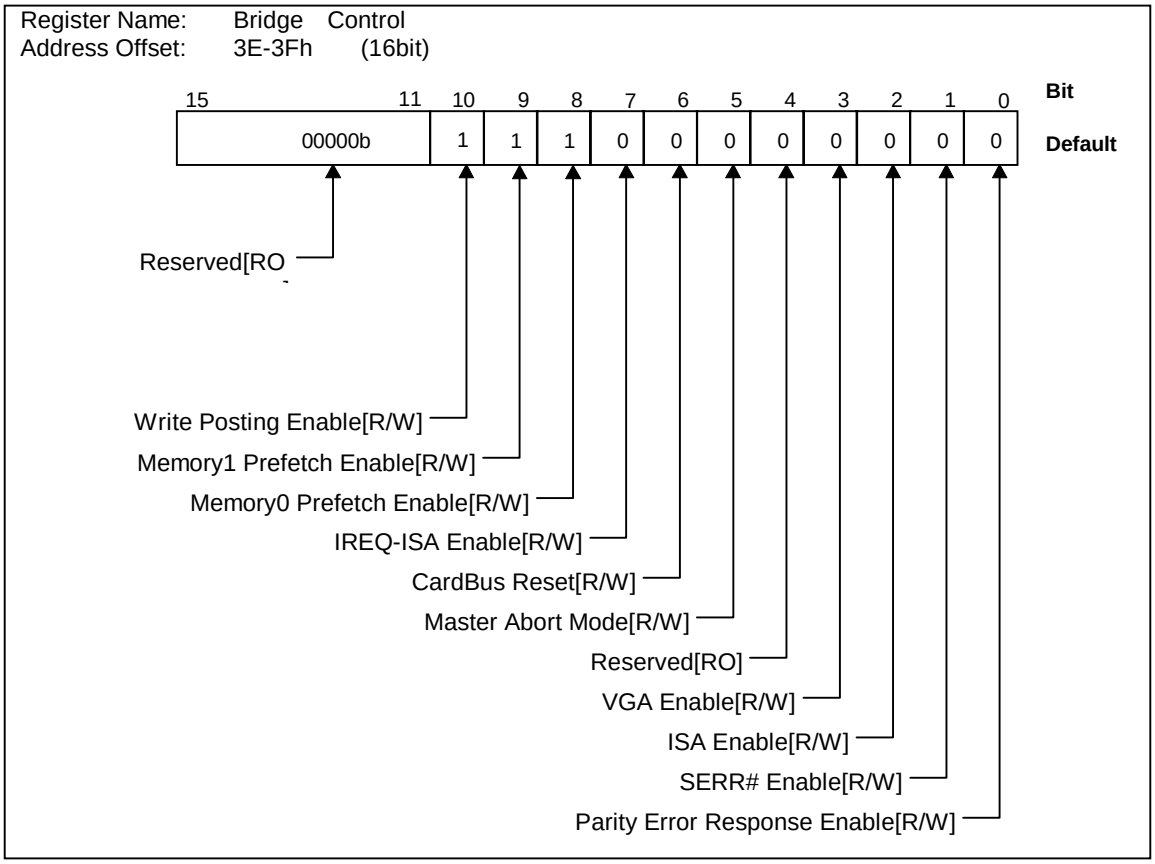


Bit	Field Name	Description
7-0	Interrupt Pin	This field is read-only and returns 01h.

5.4.31 Bridge Control register

Register Name :	Bridge Control
Address Offset :	3Eh-3Fh(16bit)
Default :	0700h
Access :	R/W

The Bridge Control register provides control over the 5C475's bridging functions. Each bit in this register adheres to the definitions in the YENTA Specification Rev. 2.2.



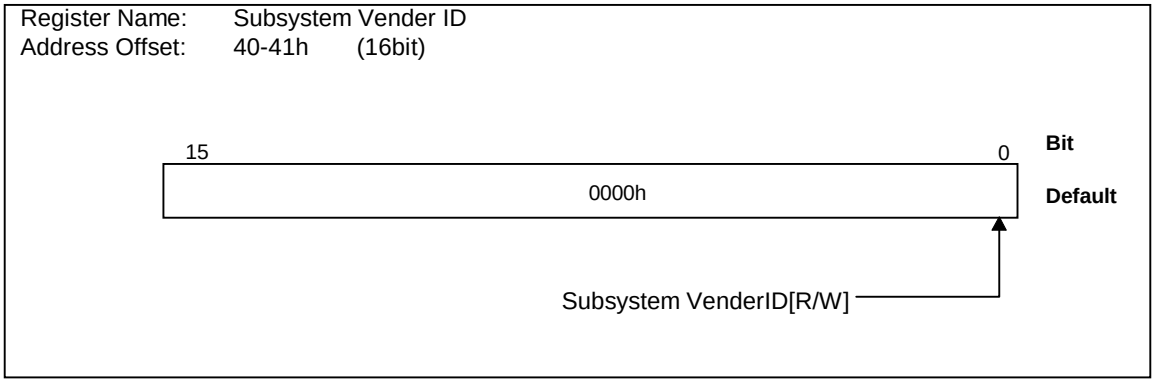
Bit	Field Name	Description
15-11	Reserved	This field is read-only and returns zeros. Writing to this field has no effect.
10	Write Posting Enable	This bit enables posting of Write data to and from the socket. If this bit is not set, the bridge must drain any data in its buffers before accepting data for or from the socket. Each data word must then be accepted by the target before the bridge can accept the next word from the source master. The bridge must not release the source master, until the last word is accepted by the target. Operating with write posting disabled will inhibit system performance. This bit is encoded as : 0 : Write Posting Disabled 1 : Write Posting Enabled (default)
9	Memory 1 Prefetch Enable	This bit specifies whether the memory window #1 is prefetchable or non-prefetchable. This bit is encoded as : 0 : the memory window #1 is non-prefetchable. 1 : the memory window #1 is prefetchable. The default after reset is one.
8	Memory 0 Prefetch Enable	This bit specifies whether the memory window #0 is prefetchable or non-prefetchable. This bit is encoded as : 0 : the memory window #0 is non-prefetchable. 1 : the memory window #0 is prefetchable. The default after reset is one.
7	IREQ-ISA Enable	This bit controls the function interrupt output pins for the PC Card-16/32. When this bit is set to one, the IREQ# interrupt is routed to the ISA system interrupt pins IRQ[15:3] that are indicated by the Interrupt General Control register. When it is set to zero, the function interrupt is routed to INTA# that is the PCI interrupt pin. The default after reset is zero.
6	CardBus Reset	When this bit is set to one, the 5C475 assert and hold CRST#. When this bit is cleared, they deassert CRST#. This bit can be set by software. It can also be set by hardware when the 5C475 executes the power down sequence. CRST# is a wired-OR of this bit and PCIRST#.
5	Master Abort Mode	When the 5C475 is a Master, this bit controls the behavior of the 5C475 when a master abort occurs on either PCI or CardBus interface. When this bit is cleared and a master abort occurs, the 5C475 returns ones on the read transaction and annuls the data on the write transaction. When this bit is set to one, the 5C475 signals a target abort to the requesting master when the corresponding transaction on the opposite bus terminates with a master abort without completing the transaction on the source side (reads and non-posted writes), and asserts SERR# on the PCI bus when the transaction on the source side and SERR# is enabled in the Command register. The default after reset is zero.
4	Reserved	This bit is read-only and returns zero. Writing to this bit has no effect.
3	VGA Enable	This bit controls the 5C475's response to VGA compatible addresses. When the VGA enable bit is set, the 5C475 forward transactions in the following ranges to the CardBus interface. Memory : 000A0000h to 000BFFFFh I/O : AD[9:0] = 3B0h to 3BBh, 3C0h to 3DFh (inclusive of ISA address aliases - AD[15:10] are not decoded.) On the other hand, the 5C475 make no response to transactions in the same ranges from the CardBus interface. The forwarding of these addresses is affected by the I/O and Memory Enable bit in the Command register. The default after reset is zero.
2	ISA Enable	This bit controls the RIL5C476/478's access to ISA compatible addresses that adhere to the first 64 Kbytes of PCI I/O space. When the ISA Enable bit is set, the 5C475 forward the only first 64 Kbytes from the PCI to the CardBus and block forwarding the last 768 bytes in 1 K block. In the opposite direction (CardBus to PCI) I/O transactions, the last 768 bytes in 1K block are forwarded. The default after reset is zero.

Bit	Field Name	Description
1	SERR# Enable	This bit controls whether or not the 5C475 forward an assertion of CSERR# on the CardBus interface to SERR# on the PCI interface.. 0 : CSERR# is not forwarded to PCI. 1 : CSERR# is forwarded to PCI. The default after reset is zero.
0	Parity Error Response Enable	This bit controls the 5C475's response to parity errors on the CardBus interface. 0 : Parity errors are ignored. 1 : Parity errors are reported . The default after reset is zero.

5.4.32 Subsystem Vendor ID register

Register Name :	Subsystem Vendor ID
Address offset :	40h-41h(16bit)
Default :	0000h
Access :	R/W

The 5C475 supports Subsystem Vendor ID register in order to correspond to the PC 97 Design requirements. It is possible to write into this register from the system by setting Subsystem ID Write Enable bit (Bit6 in the Misc Control register). This register is not initialized by either PCIRST# or the reset generated by the power state transition from D3 to D0 independently of the PME_En bit, as long as the power state is D3.

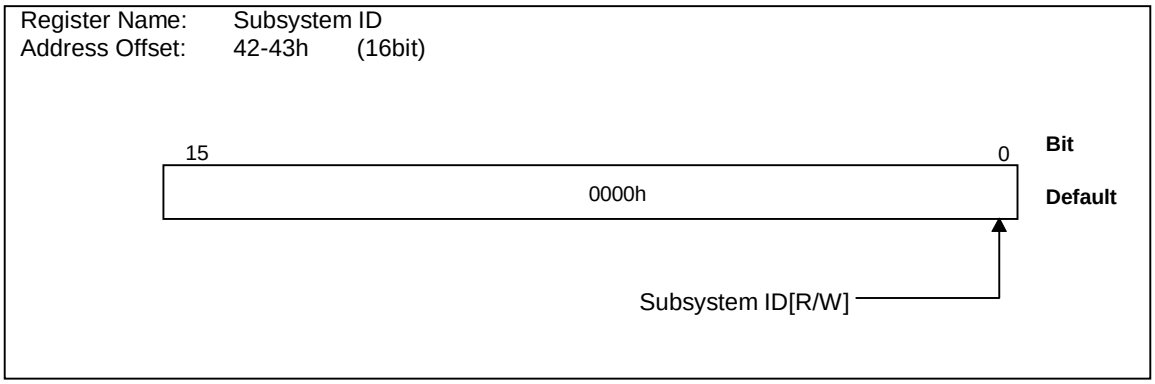


Bit	Field Name	Description
15-0	Subsystem Vender ID	It is possible to write into this field from the system by setting Subsystem ID Write Enable bit (Bit6 in the Misc Control register). The default after reset is zeros.

5.4.33 Subsystem ID register

Register Name :	Subsystem ID
Address Offset :	42h-43h(16bit)
Default :	0000h
Access :	R/W

The 5C475 supports Subsystem ID register in order to correspond to the PC 97 Design requirements. It is possible to write into this register from the system by setting Subsystem ID Write Enable bit (Bit6 in the Misc Control register). This register is not initialized by either PCIRST# or the reset generated by the power state transition from D3 to D0 independently of the PME_En bit, as long as the power state is D3.

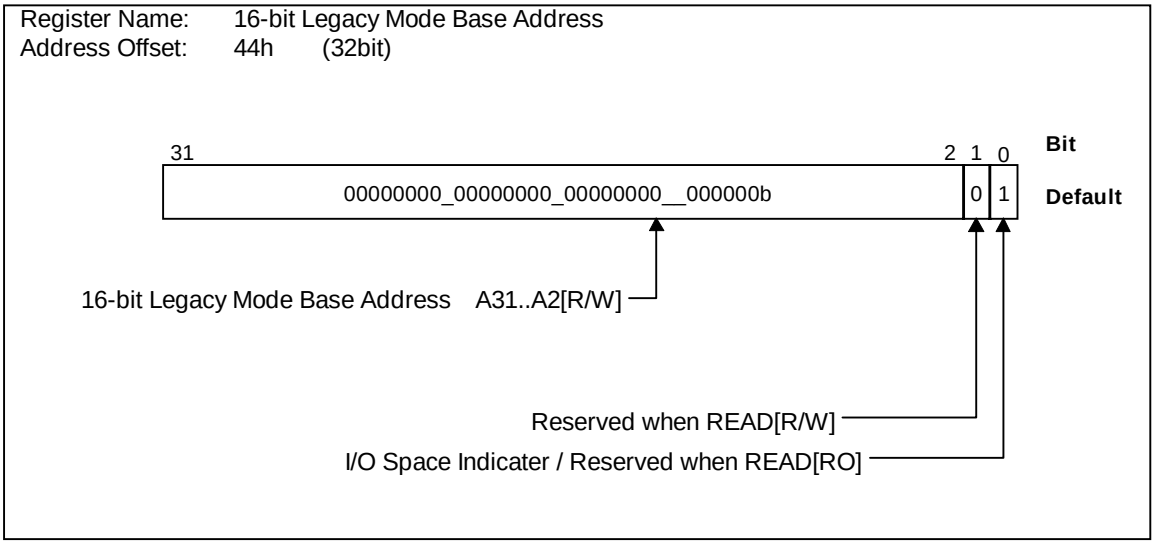


Bit	Field Name	Description
15-0	Subsystem ID	It is possible to write into this field from the system by setting Subsystem ID Write Enable bit (Bit6 in the Misc Control register). The default after reset is zeros.

5.4.34 16-bit Legacy Mode Base Address register

Register Name :	16-bit Legacy Mode Base Address
Address Offset :	44h(32bit)
Default :	0000_0001h
Access :	R/W

The 16-bit Legacy Mode Base Address register indicates the base address to map the Legacy Port on the PCI Card-16. Normally, this register is set to 3E0h or 3E2h in order to keep corresponding to the PCIC. The bits[31:2] are read/write, but the bits[1:0] are hardwired to 01b when read. It dose not respond to PCI cycles unless specifically loaded with a non-zero address after PCIRST# is deasserted.

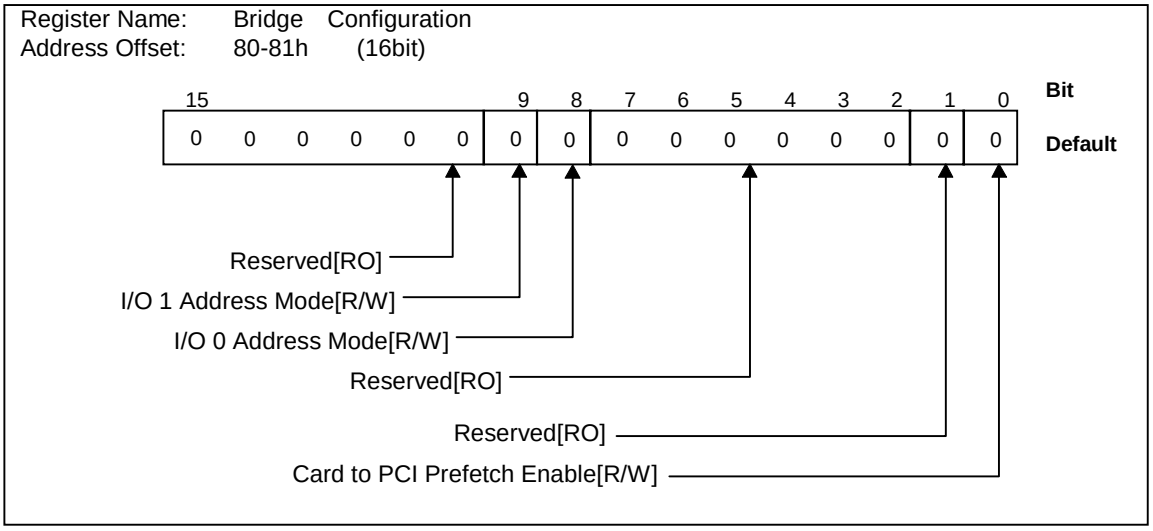


Bit	field Name	Description
31-2	16-bit Legacy Mode Base Address A31..A2	This field indicates the base address to map INDEX/DATA port (3E0h,3E1h) corresponding to the PCIC when the PCI Card-16 is inserted. This field is read/write, and writing to this field has no effect. The default after reset is zero.
1	Reserved	It is possible to write a data in this field, therefore this register can be 03E0h or 03E2h. This field returns zero when read.
0	I/O Space Indicator	This bit indicate whether or not the Card Control register space indicated by the Base Address register is I/O space. This bit returns one when read.

5.4.35 Bridge Configuration register

Register Name :	Bridge Configuration
Address Offset :	80h-81h(16bit)
Default :	0000h
Access :	R/W

The Bridge Configuration register is used to control the bridge functions specific to the 5C475 like an I/O addressing mode and Prefetchabel memory transactions from CardBus to PCI bus. Each socket has its own Bridge Configuration register.

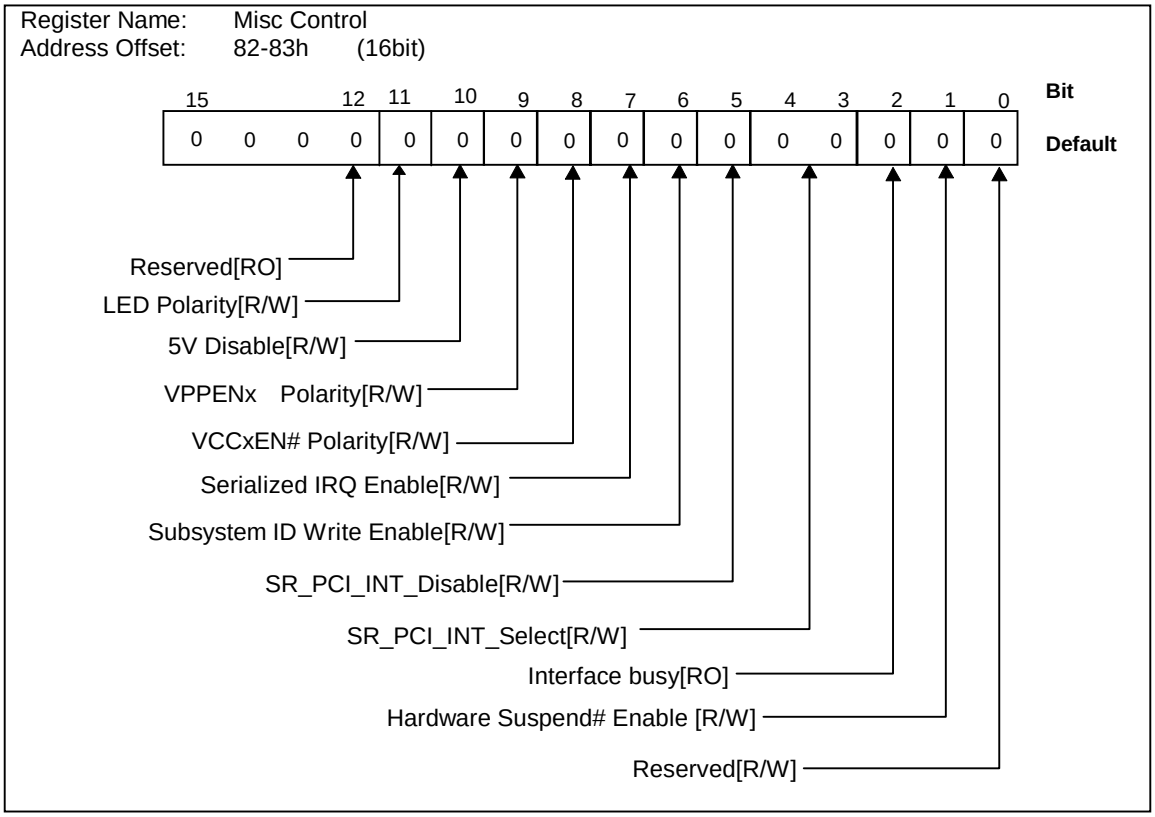


Bit	Field Name	Description
15-10	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
9	I/O 1Address Mode	This bit controls the address size of I/O window #1. When this bit is set to one, the I/O Base #1 Upper register and the I/O Limit #1 Upper register are enabled. When this bit is set to zero, the I/O Base #1 Upper register and the I/O Limit #1 Upper register are disabled, and the I/O transaction is forwarded only when the upper 16-bit address[31:16] is zero. The default after reset is zero.
8	I/O 0Address Mode	This bit controls the address size of I/O window #0. When this bit is set to one, the I/O Base #0 Upper register and the I/O Limit #0 Upper register are enabled. When this bit is set to zero, the I/O Base #0 Upper register and the I/O Limit #0 Upper register are disabled, and the I/O transaction is forwarded only when the upper 16-bit address[31:16] is zero. The default after reset is zero.
7-2	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
1	Reserved	This bit is reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
0	Card to PCI Prefetch Enable	When this bit is one, Read Prefetch is enabled from CardBus to PCI bus. The default after set is zero.

5.4.36 Misc Control register

Register Name :	Misc Control
Address Offset :	82h-83h(16bit)
Default :	0000h
Access :	R/W

The Misc Control register controls the power-down mode of the 5C475, the polarity of the card power enable signal, Serialized IRQ and Subsystem ID write signals enable/disable. This register is initialized by only PCIRST# independently of the power state.

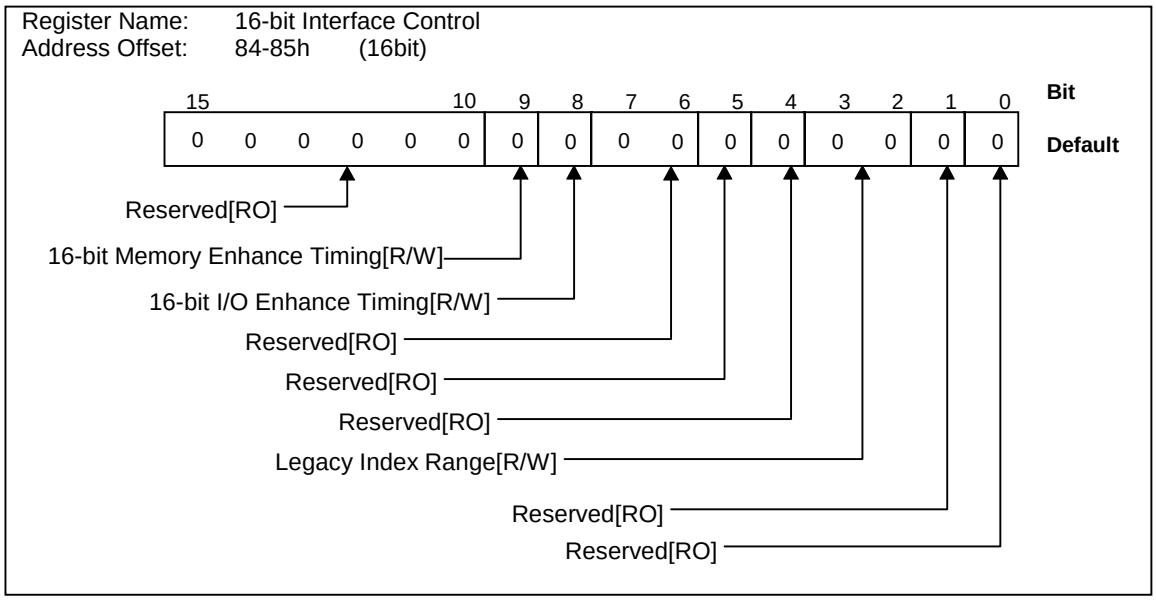


Bit	Field Name	Description
15-12	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
11	LED Polarity	This bit controls the polarity of LED signal. The default is zero and “low” active. When this bit is set to one, LED signal is “high” active.
10	5V Disable	In the card supplied 5V/3.3V, 5V is disabled when this bit is set.
9	VPPENx Polarity	This bit controls the polarity of VPPEN1 and VPPEN0 signals. When this bit is set to one, VPPEN1 and VPPEN0 are “low” active signals. When this bit is cleared, VPPEN1 and VPPEN0 are “high” active signals. The default after reset is zero.
8	VCCxEN# Polarity	This bit controls the polarity of VCC5EN# and VCC3EN# signals. When this bit is set to one, VCC5EN# and VCC3EN# are “high” active signals. When this bit is cleared, VPPEN1 and VPPEN0 are “high” active signals. The default after reset is zero.
7	SRIRQ Enable	When this bit is set, the serialized IRQ mode is enabled. IRQ9 is assigned as SIRQ# signal and IRQ14,15 is reassigned as AZVEN#, BZVEN# that is a ZV port control signal. The default after reset is zero.
6	Subsystem ID Write Enable	When this bit is set to one, Writing to Subsystem Vendor ID and Subsystem ID is enabled. The default after reset is zero.
5	SR_PCI_INT_Disable	When this bit is set to zero, The 5C475 can insert the frame of INTA#, INTB#, INTC#, and INTD#(PCI Interrupt signals) following IOCHK# frame. The default after reset is zero.
4-3	SR_PCI_INT_Select	This field indicates which of PCI_INT# signals outputted from SRIRQ# is selected. 00b INTA# (Default) 01b INTB# 10b INTC# 11b INTD#
2	Interface Busy	This field is read-only. When this bit is set to one, the card interface is busy. Returns zero when the internal buffers are empty. The default after reset is zero.
1	Hardware Suspend# Enable	When this bit is set to 1, SPKROUT# pin is reassigned as Hardware Suspend# input. Once Hardware Suspend# is asserted, all PCI interface signals are disabled and VCC_PCI can be powered off. This bit can not be reset by PCIRST#. Default is zero.
0	Reserved	This bit are reserved for future use. This field is read/write and returns zero when read. Writing to this field has no effect.

5.4.37 16-bit Interface Control register

Register Name :	16-bit Interface Control
Address Offset :	84h-85h(16bit)
Default :	0000h
Access :	R/W

The 16-bit Interface Control register is used to set 16-bit interface timing and the PCIC compatible mode.

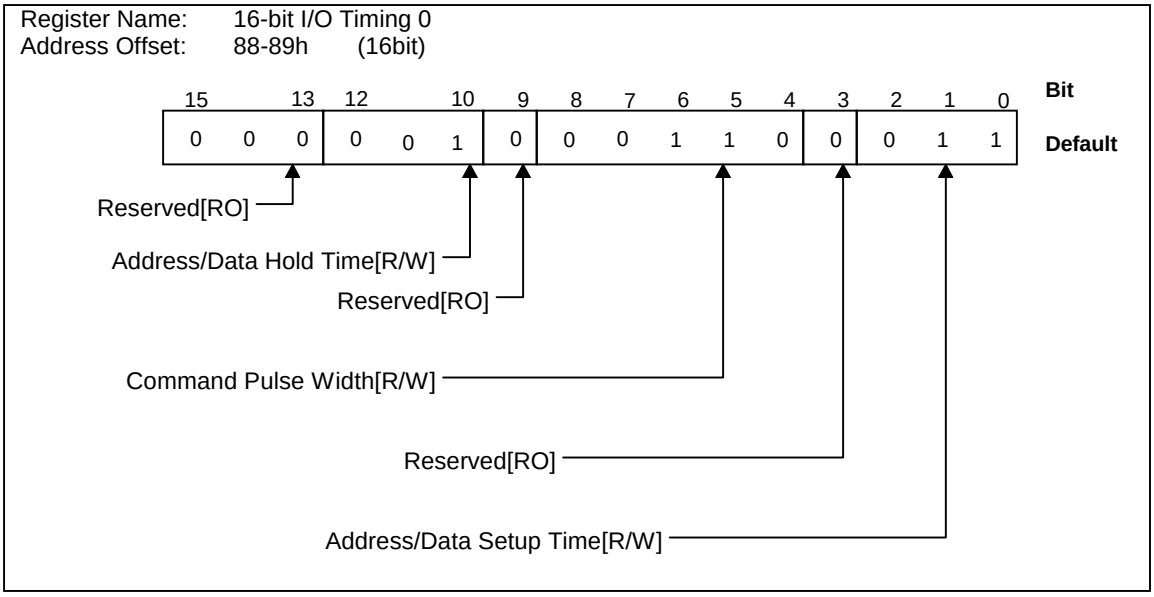


Bit	field Name	Description
15-10	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
9	16-bit Memory Enhance Timing	When this bit is set to one, the 16-bit memory enhanced timing is enabled. 16-bit memory access timing is determined by 16-bit Memory Timing #0 register. When this bit is reset to zero, 16-bit memory access timing is reset to the default condition. The default after reset is zero.
8	16-bit I/O Enhance Timing	When this bit is set to one, the 16-bit I/O enhanced timing is enabled. 16-bit I/O access timing is determined by 16-bit I/O Timing #0 register. When this bit is reset to zero, 16-bit I/O timing is reset to the default condition. The default after reset is zero.
7-4	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
3-2	Legacy Index Range	This bit defines the index range which is accessed through PCIC compatible I/O port 3E0 or 3E2. index range 00 : 00h to 3Fh 01 : 40h to 7Fh 10 : 80h to BFh 11 : C0h to FFh Default is zero.
1-0	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.

5.4.38 16-bit I/O Timing 0 register

Register Name :	16-bit I/O Timing 0
Address Offset :	88h-89h(16bit)
Default :	0463h
Access :	R/W

16-bit I/O access timing parameters are independently configured for each socket by programming this register.

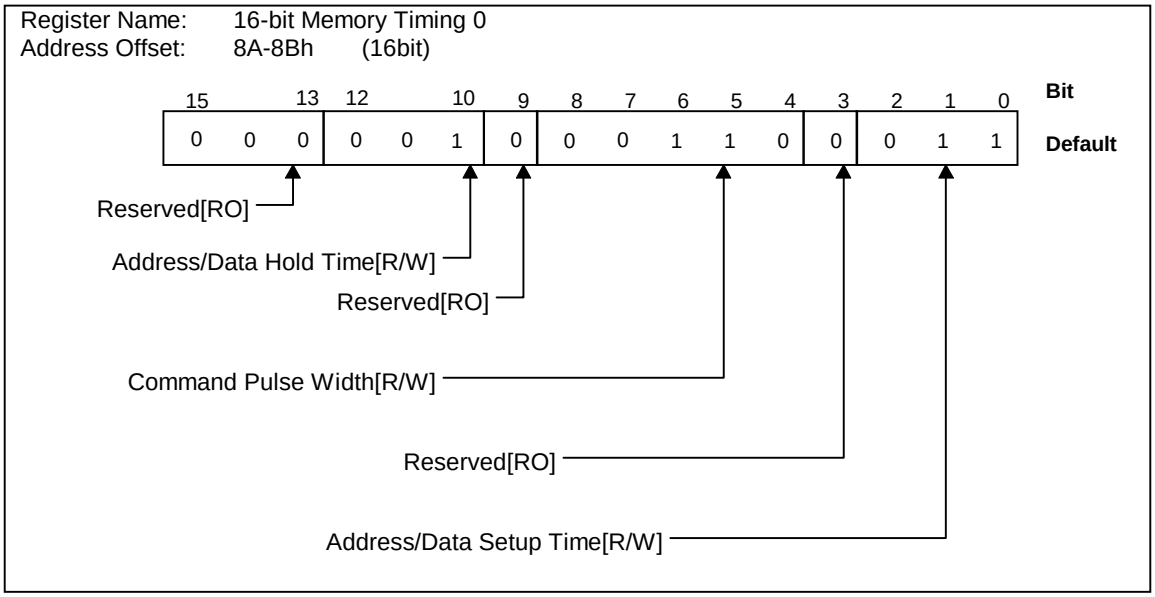


Bit	Field Name	Description
15-13	Reserved	These bits are reserved for future use. This field is read-only and returns zeros when read. Writing to this field has no effect.
12-10	Address/Data Hold Time	This field indicates the address hold time and the data hold time of 16-bit I/O cycle. The hold time can be set in a timer granularity of PCICLK. The default after reset is 001b.
9	Reserved	This bit is reserved for future use. This bit is read-only and returns zero when read. Writing to this bit has no effect.
8-4	Command Pulse Width	This field indicates the command pulse width of 16-bit I/O cycle for IORD# and IOWR#. The pulse width can be set in a timer granularity of PCICLK. The default after reset is 00110b.
3	Reserved	This bit is reserved for future use. This bit is read-only and returns zero when read. Writing to this bit has no effect.
2-0	Address/Data Setup Time	This field indicates the address setup time and the data setup time of 16-bit I/O cycle. The setup time can be set in a timer granularity of PCICLK. The default after reset is 011b.

5.4.39 16-bit Memory Timing 0 register

Register Name :	16-bit Memory Timing 0
Address offset :	8Ah-8Bh(16bit)
Default :	0463h
Access :	R/W

16-bit Memory access timing parameters are independently configured for each socket by programming this register.



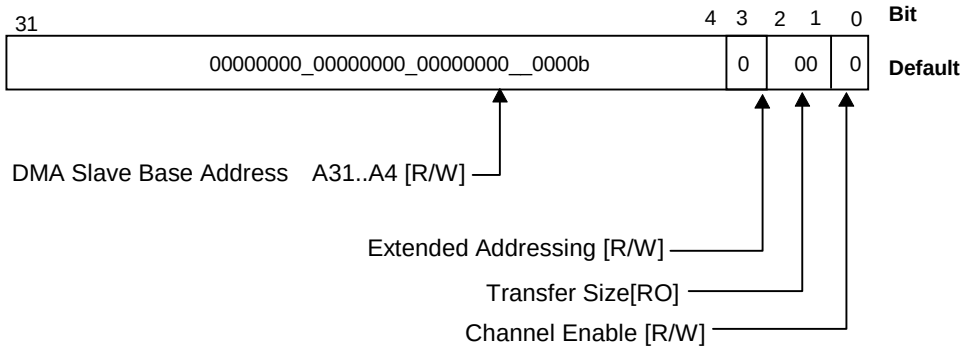
Bit	Field Name	Description
15-13	Reserved	These bits are reserved for future use. This field is read-only and returns zeros when read. Writing to this bit has no effect.
12-10	Address/Data Hold Time	This field indicates the address hold time and the data hold time of 16-bit memory cycle. The hold time can be set in a timer granularity of PCICLK. The default after reset is 001b.
9	Reserved	This bit is reserved for future use. This bit is read-only and returns zero when read. Writing to this bit has no effect.
8-4	Command Pulse Width	This field indicates the command pulse width of 16-bit memory cycle for OE# and WE#. The pulse width can be set in a timer granularity of PCICLK. The default after reset is 00110b.
3	Reserved	This bit is reserved for future use. This bit is read-only and returns zero when read. Writing to this bit has no effect.
2-0	Address/Data Setup Time	This field indicates the address setup time and the data setup time of 16-bit memory cycle. The setup time can be set in a timer granularity of PCICLK. The default after reset is 011b.

5.4.40 DMA Slave Configuration register

Register Name :	DMA Slave Configuration
Address Offset :	90h-93h(32 bit)
Default :	0000_0000h
Access :	R/W

The DMA Slave Configuration register indicates the base address to the distributed DMA that supports ISA-DMA functions.

Register Name: DMA Slave Configuration register
Address Offset: 90h (32bit)

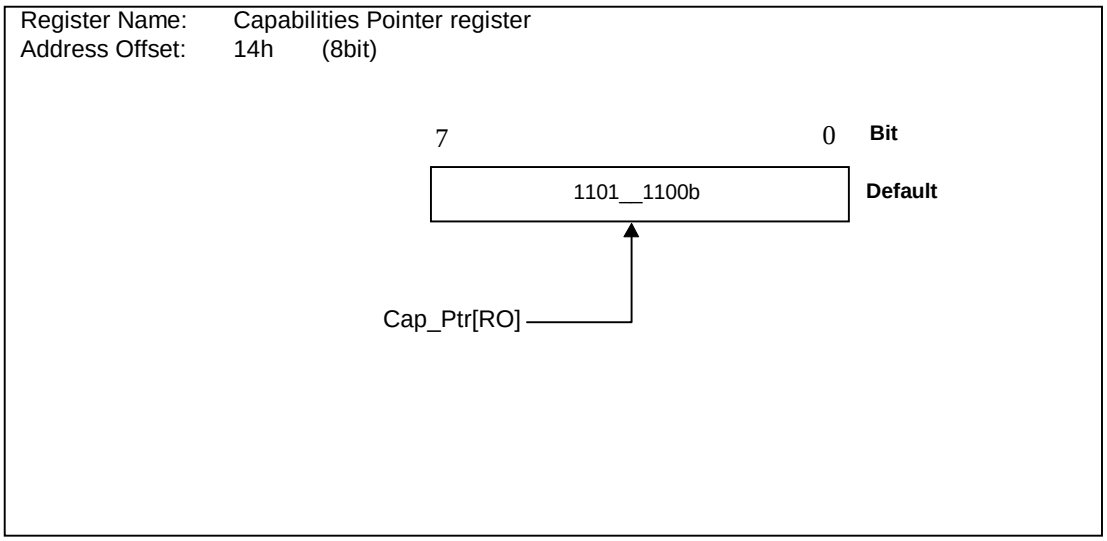


Bit	Field Name	Description
32-4	DMA Slave Base Address	This field indicates the base address [31:4] that defines the address range of the distributed DMA. The default after reset is zero.
3	Non Legacy Extended Addressing	When this bit is set to one, Non Legacy Extended Addressing mode is enabled. That is the address space is extended to 32-bit (Base+3), and the byte count is extended to 24-bit (Base+6). The default after reset is zero.
2-1	Transfer Size	This field defined the width of the DMA transfer on the PC Card interface. 00 8 bit transfer at the PC card 01 16 bit transfer at the PC card 10 32 bit transfer at the PC card (**not allowed**) 11 reserved
0	Channel Enable	This bit enables the decoding of the base address with DMA Enable bit in the Misc Control 1 register. When this bit is set to zero, the DMA transfer is disabled. The default after reset is zero.

5.4.41 Capabilities Pointer register

Register Name :	Capabilities Pointer
Address Offset :	14h (8 bit)
Default :	DCh
Access :	RO

The Capabilities Pointer register is read-only and provides an offset into the function's PCI Configuration Space for the location of the first item in the New Capabilities List. The 5C475 supports the PCI Power Management. This register is assigned a value of 0DCh for the PCI Power Management.

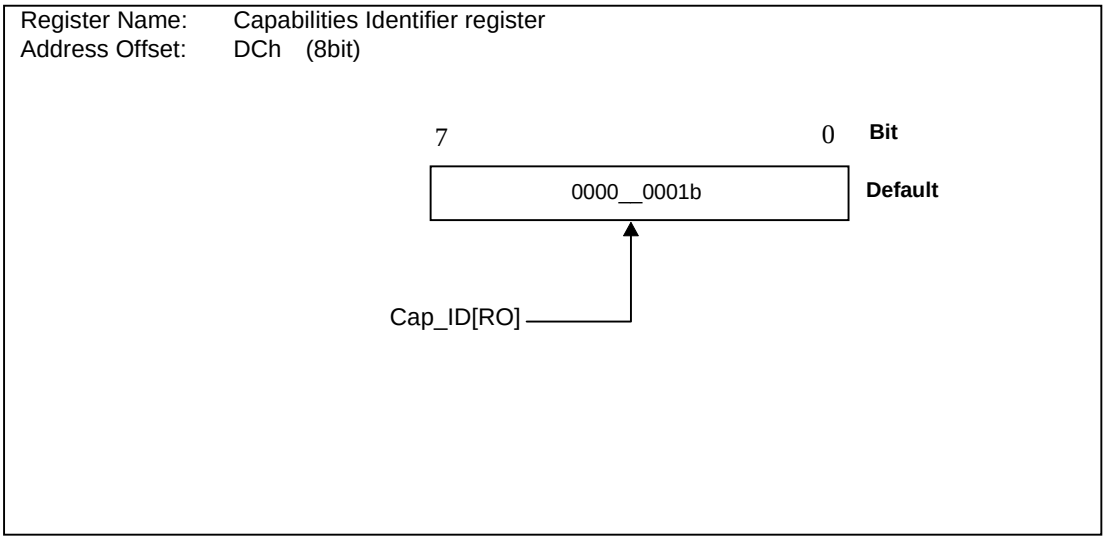


Bit	Field Name	Description
7-0	Capabilities Pointer	This field provides an offset into the function's PCI Configuration Space for the location of the first item in the New Capabilities Linked List. The 5C475 supports the PCI Power Management as a new function. This field is assigned a value of 0DCh for the PCI Power Management.

5.4.41.1 Capabilities Identifier register

Register Name :	Capabilities Identifier
Address Offset :	Cap_Ptr (DCh) (8 bit)
Default :	01h
Access :	RO

The Capabilities Identifier register is read-only and indicates only one item in the linked list is the registers defined for the PCI Power Management. This register is assigned the ID of 01h.



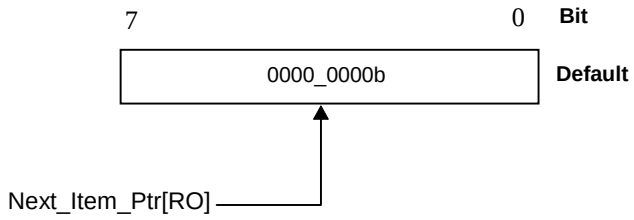
Bit	Field Name	Description
7-0	Capabilities Identifier	This field indicates the 5C475 support the PCI Power Management as a new function. This field is read-only and assigned the ID of 01h.

5.4.41.2 Next Item Pointer register

Register Name :	Next Item Pointer
Address Offset :	Cap_Ptr + 1 (DDh) (8 bit)
Default :	00h
Access :	RO

The Next Item Pointer register is read-only and indicates the location of the next item in the function's capability list. The 5C475 dose not support items in the list except the PCI Power Management. So, this field is assigned a value of 00h.

Register Name: Next Item Pointer register
Address Offset: DDh (8bit)

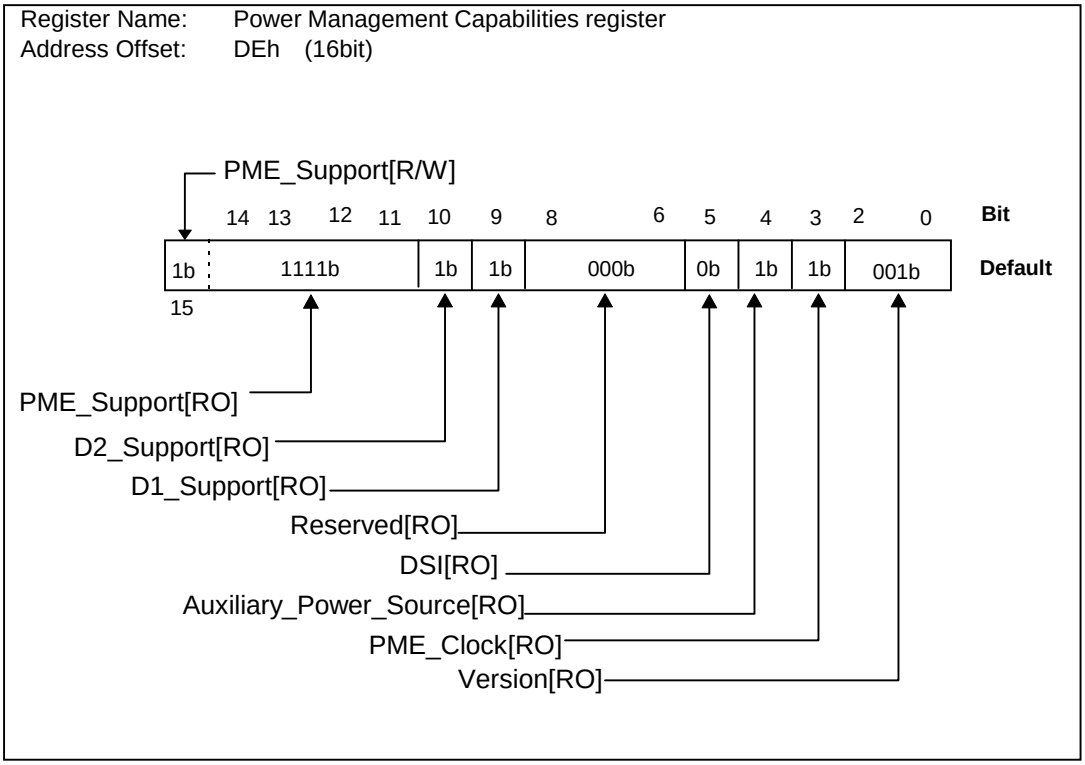


Bit	Field Name	Description
7-0	Next Item Pointer	This field indicates the location of the next item in the function's capability list. The 5C475 dose not support items in the list except the PCI Power Management. This field is read-only and assigned a value of 00h.

5.4.41.3 Power Management Capabilities register

Register Name :	Power Management Capabilities
Address Offset :	Cap_Ptr + 2 (DEh)(16 bit)
Default :	FE19h
Access :	RO

The Power Management Capabilities register is read-only and provides information on the capabilities of the function related to the PCI Power Management.

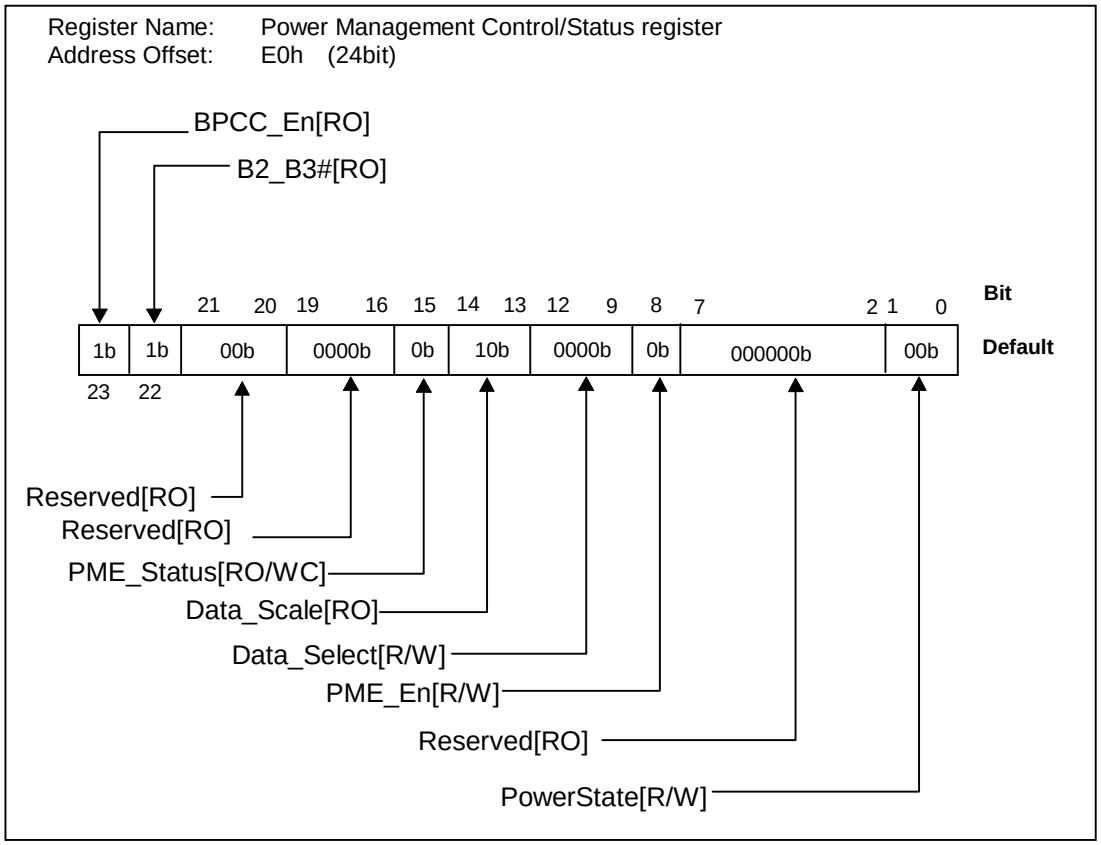


Bit	Field Name	Description
15 14-11	PME_Support	This five bit field indicates the power states that the device supports asserting PME#. A value of 0 for any bit indicates that the function is not capable of asserting the PME# signal from that power state. XXXX1b - PME# can be asserted from **D0** (bit 11) XXX1Xb - PME# can be asserted from **D1** (bit 12) XX1XXb - PME# can be asserted from **D2** (bit 13) X1XXXb - PME# can be asserted from **D3**hot (bit 14) 1XXXXb - PME# can be asserted from **D3**cold (bit15) Bit 15 is set to one if PME# can be asserted by the supply of auxiliary power, even if the PCI Vcc is turned off. If the auxiliary power is not supported, this bit must be set to zero because PME# is not asserted. The PME# signal indicates Wakeup events that include a “Ring Indication” from a Modem or the receipt of special packet by a Network card. When once PME# is asserted, it is kept at the state until Status bit (bit 15) is cleared or Enable bit (bit 8) is reset in the Power Management Control/Status register. In the 5C475, the RI_OUT# signal can use as the PME# signal. Therefore all bits in this field return one.
10	D2_Support	Returns one, because the 5C475 supports the D2 Power Management State.
9	D1_Support	Returns one, because the 5C475 supports the D1 Power Management State.
8-6	Reserved	Reserved. Returns zeros.
5	DSI	This Device Specific Initialization bit is set to one when a device specific device driver is required to reinitialize a device after it leaves the D3 state. Returns zero as it is not necessary to reinitialize in the 5C475.
4	Auxiliary_Power_ Source	When this bit is a “1” it indicates that support for PME# in D3cold requires auxiliary power supplied by the system by some means. A “0” in this bit indicates that the function supplies its own auxiliary power source. This bit returns one because the 5C475 needs the auxiliary power in D3cold.
3	PME clock	When this bit is a “1” it indicates that the function relies on the presence of the PCI clock for PME# operation. When this bit is a “0” it indicates that no PCI clock is required for the function to generate PME#. This bit returns one because the 5C475 needs PCI clock to generate PME# when the power management event is caused by Ready/Busy change or Battery Warning. The 5C475 can generate PME# without PCI clock if PME is caused by Card detect change or Card status change.
2-0	Version	The 5C475 has 4 bytes of general purpose Power Management registers implemented as described in PCI Bus Power Management specification Rev1.0. These bits usually return 001b.

5.4.41.4 Power Management Control/Status register

Register Name :	Power Management Control/Status
Address Offset :	Cap_Ptr +4 (E0h)(24 bit)
Default :	C04000h
Access :	R/W

The Power Management Control/Status register is used to control the current power state of the PCI function and inform the status information. The contents of this register are not affected by the internally generated reset caused by the transition from D3 to D0.

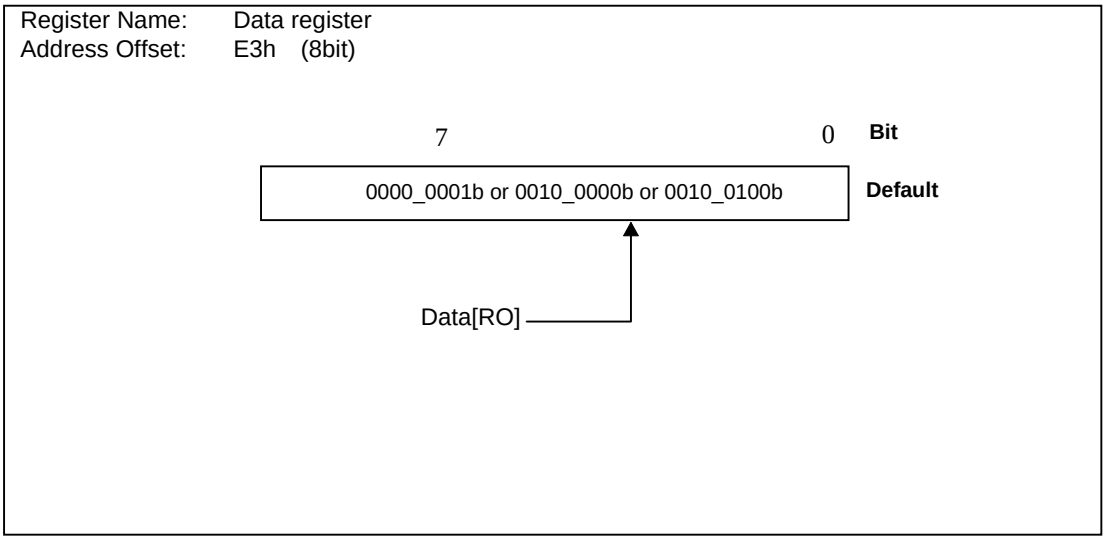


Bit	Field Name	Description
23	BPCC_En	This is Bus Power Clock Control Enable bit. Returns one as the bus power and clock control mechanism in the CardBus follows the power managing state of the 5C475.
22	B2_B3#	The state of this bit determines the action that is to occur as a direct result of programming the function to D3hot. A “1” indicates that when the bridge function is programmed to D3hot, its secondary bus’s PCI clock will be stopped (B2). A “0” indicates that when the bridge function is programmed to D3hot, its secondary bus will have its power removed (B3). Returns one as the CardBus clock will be stopped when the 5C475 function is programmed to D3hot.
21-16	Reserved	Reserved. Return zeros when read.
15	PME_Status	This bit is set when the function normally asserts the PME# signal independent of the state of the PME_En bit (bit 8). Writing a one to this bit clears it and causes the function to stop asserting a PME# (if enabled). Writing a zero has no effect. The default after reset is zero.
14-13	Data_Scale	This two bit read-only field indicates the scaling factor to be used when interpreting the value of the Data register. Returns 10b as the 5C475 offers the information of power consumed in a 10mW step.
12-9	Data_Select	This four bit field is used to select which data is reported through the Data register and Data_Scale field. The default after reset is zero. 0000 D0 power consumed 0001 D1 power consumed 0010 D2 power consumed 0011 D3 power consumed 0100 D0 power dissipated 0101 D1 power dissipated 0110 D2 power dissipated 0111 D3 power dissipated 1xxx Reserved
8	PME_En	When the D0 state is set, the function is enabled to assert PME# when this bit is set to one. The assertion of PME# is disabled when this bit is cleared. The default after reset is zero. The following registers are not initialized by either PCIRST# or the reset generated by the power state transition from D3 to D0 as long as the power state is D3 and PME Enable bit is set to ”1”. Address — Register Name — Bit 000h — Socket Event — [3:0] 004h — Socket Mask — [3:0] 008h — Socket Present State — [11,10,5,4] 010h — Socket Control — [6:4] 802h — Power Control — [7:2] 804h — Card Status Change — [3:0] 805h — Card Status Change Interrupt Configuration — [3:0] 82Fh — Misc Control 1 — [0] DEh — Power Management Capabilities — [15] E0h — Power Management Control/Status — [15, 8] And also, each bit of the following registers is initialized under the each different conditions. 1. It is initialized by only PCIRST# independently of the power state. 82h — Misc Control — [15:0] 2. It is initialized by PCIRST# when the power state is selected except D3 40h — Subsystem Vender ID — [15:0] 42h — Subsystem ID — [15:0] *The rest of bits(except the above bits) are initialized by the internal reset or the assertion PCIRST# under no conditions.
7-2	Reserved	Reserved. Return zeros when read.
1-0	PowerState	This field is used to set the function into a new power state. The definition of the field values is : 00b - D0 01b - D1 10b - D2 11b - D3hot The default after reset is zeros.

5.4.41.5 Data Register

Register Name :	Data
Address Offset :	Cap_Ptr + 7 (E3h)(8 bit)
Default :	01h or 20h or 24h
Access :	RO

The Date register is read-only and provides a maximum value of the power consumed for each function from the PCI device by using with Data_Select bit fields and Data_Scale bit field.



Bit	Field Name	Description
7-0	Data	This read-only bit field provides the maximum value of the power consumed by the 5C475 for each function from the PCI device. The maximum value of the power consumed is 10mW times the value of Data_Scale bit field. The 5C475 returns the following value. D0 power state : 0010 0100b (360mW) D1 power state : 0010 0000b (320mW) D2 power state : 0000 0001b (10mW) D3 power state : 0000 0001b (10mW)

6 CARDBUS(PC CARD-32) SOCKET STATUS CONTROL REGISTERS

6.1 Overview

CardBus Socket Status/Control registers manage changed events, remote wakeup events, PC Card insertion/removal, and status information about the PC Card in the socket. These registers are used for PC Card-32 as well as PC Card-16.

6.2 Register Space mapping

PC Card Control Register Base Address register points to the 4Kbyte memory mapped I/O space that contains both the PC Card-32 and PC Card-16 Status and Control registers. Socket Status/Control Registers for PC Card-32 are placed in the bottom 2KByte of the 4KByte and start at offset 000h. The registers for PC Card-16 are placed in the upper 2KByte and start at offset 800h.

6.3 Register Configuration

Each socket has CardBus Socket Status/Control registers which consist of six DWORD registers. One set of registers are described in the following sections, with the address offset for each socket. Address offset 014h through 7FCh are assigned to the reserved registers. The reserved registers return 00000000h when read. Writing to the reserved registers has no effect.

Register Space Name: CardBus Socket Status / Control Register Space

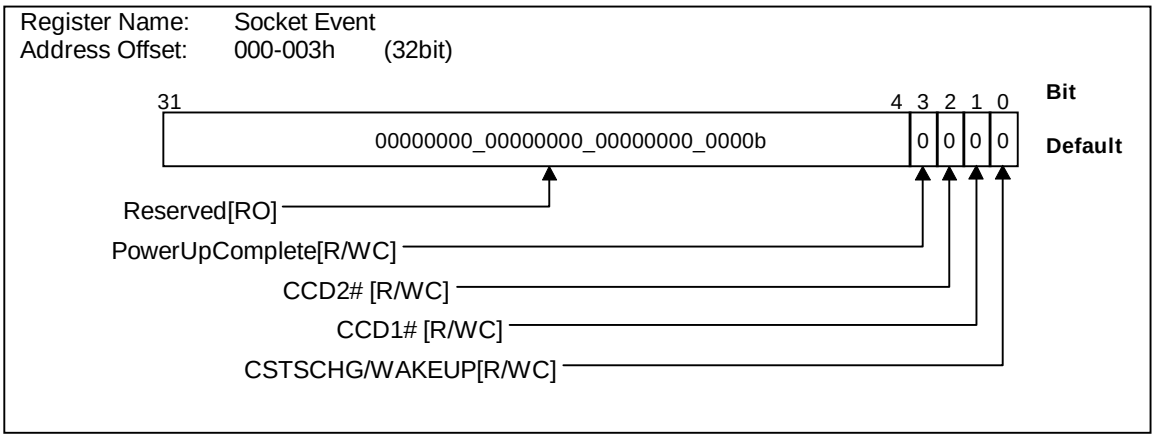
31 24	23 16	15 8	7 0	Bit
Socket Event				000h
Socket Mask				004h
Socket Present State				008h
Socket Event Force				00Ch
Socket Control				010h
Reserved				014h ~ 7FCh

6.4 Register Description

CardBus Socket Status/Control registers manage status changed events, remote wakeup events, PC Card insertion/removal, and status information about the PC Card in the socket. These registers are used for PC Card-32 as well as PC Card-16.

6.4.1 Socket Event register

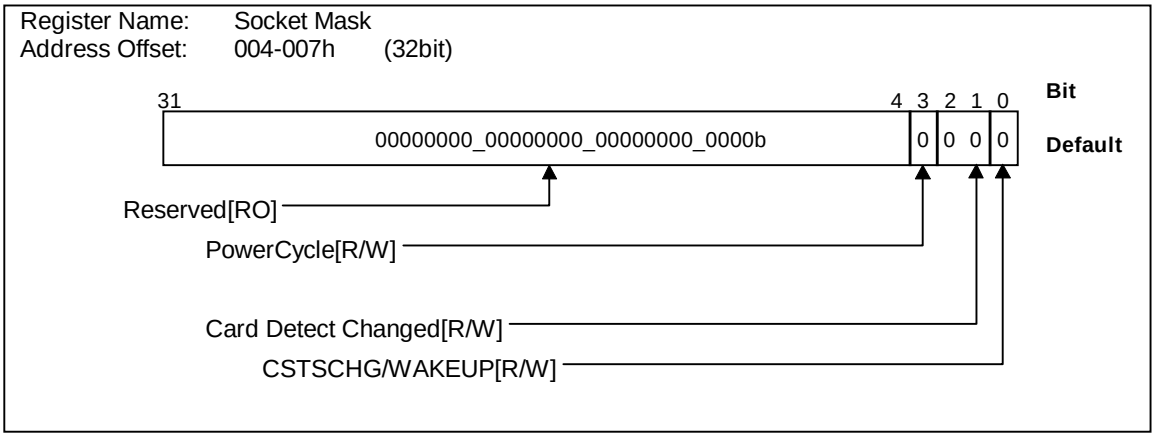
The Socket Event register indicates a change in socket status has occurred. These bits do not indicate what the change is, only that one has occurred. Software must read the Socket Present State register for current status. Each bit in this register can be cleared by writing a one to that bit. These bit can be set to a one by software through writing a one to the corresponding bit in the Socket Event Force register. All bits in this register are cleared by PCIRST#. They may be immediately set again, if when coming out of CRST# the bridge finds the status unchanged (i.e., CSTSCHG reasserted or Card Detects is still true). Software needs to clear this register before enabling interrupts. If it is not cleared, when interrupts are enabled an interrupt will be generated based on any bit set but not masked.



Bit	Field Name	Description
31-4	Reserved	These bits are reserved for future use. This field is read-only and returns zeros. Writing to this field has no effect.
3	PowerUpComplete	This bit is set when the 5C475 detected to complete powering up the PC Card-32 socket. The Socket Present State register should be read to determine whether or not the voltage requested was actually applied. This bit is cleared by writing a one. The default after reset is zero. This bit has no meaning when the 16-bit card is installed.
2	CCD2#	This bit is set whenever the CCD2# field in the Present State register changes state. This bit is cleared by writing a one. The default after reset is zero.
1	CCD1#	This bit is set whenever the CCD1# field in the Present State register changes state. This bit is cleared by writing a one. The default after reset is zero.
0	CSTSCHG/WAKEUP	This bit is set whenever the CSTSCHG/WAKEUP# was asserted, and indicates only the assertion event. However, this bit isn't directly reflected in a status change of the CSTSCHG/WAKEUP# in the Socket Present State register, and also, it isn't directly reflected in a status of the CSTSCHG bit from the card. This bit needs to be controlled by Software. This bit is cleared by writing a one. The default after reset is zero. This bit is meaningless when the 16-bit card is installed. If STSCHG# interrupt signal from the 16-bit card was occurred, this bit will be controlled by the 16-bit Card Status/Control register.

6.5 Socket Mask register

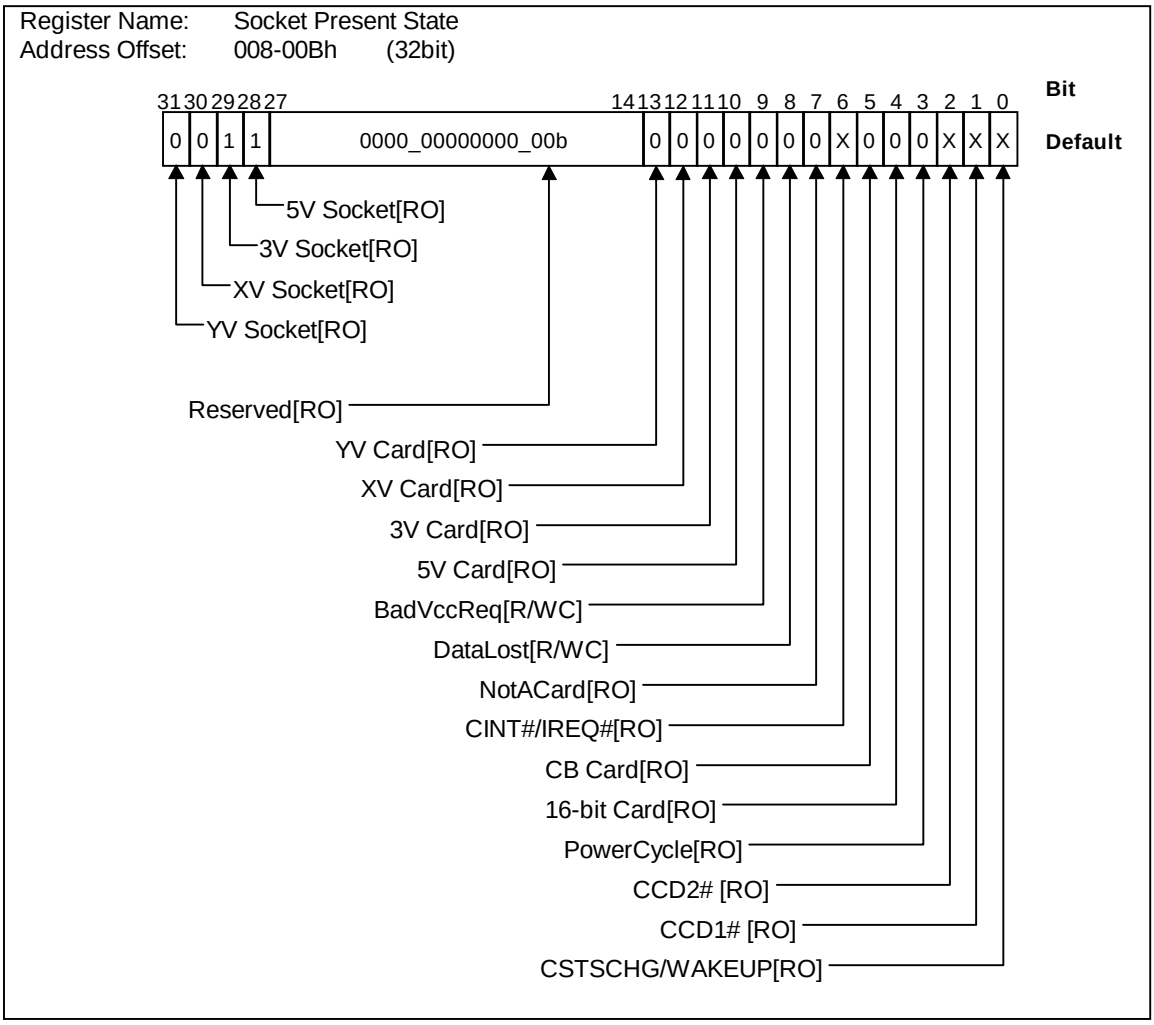
The Socket Mask register allows software to control the CardBus card events which generate a status change interrupt. If the Card Detect Changed bit is enabled at the time a card is removed, an interrupt is generated. After that, this bit is cleared automatically. This is to prevent spurious interrupts while cards are removed. If it is desired to have the bridge generate an interrupt at the time a new card is inserted, it is necessary that this bit is set again by software. This register is cleared by PCIRST#. The default after reset is zero.



Bit	Field Name	Description
31-4	Reserved	These bits are reserved for future use. This field is read-only and returns zeros. Writing to this field has no effect.
3	PowerCycle	This bit masks a status changed interrupt caused by the event that indicates the end of power up process. When cleared (0), the status changed event signaling the power up process has completed is not generated, although the PowerCycle field in the Socket Event register is set. When this bit is set by writing a one, an interrupt is generated after 256 cycles since a socket was finished powering up. The default after reset is zero.
2-1	Card Detect Changed	This field masks the CCD1# and CCD2# fields in the Socket Event register so that insertion and removal events will not cause a status changed interrupt to occur. The meaning of the bit is : 00 - Mask the CCD1# and CCD2# fields in the Socket Event register. Card insertion/removal events will not cause a status change interrupt. 01 - Undefined 10 - Undefined 11 - Unmask the CCD1# and CCD2# fields in the Socket Event register. Card insertion/removal events will cause a status change interrupt. The CCD1# and CCD2# fields in the Socket Event register are set in spite of setting of this field. The default after reset is zero.
0	CSTSCHG/WAKEUP	This bit masks a status changed interrupt of the CSTSCHG/WAKEUP. When cleared (0), the assertion of CSTSCHG/WAKEUP by the card is not cause a status changed interrupt to occur, although the CSTSCHG/WAKEUP field in the Socket Event register is set. This bit is set by writing a one, and is cleared when the socketed PC card is removed or when the 5C475 is reset. This bit has no meaning when the 16-bit card is inserted.

6.5.1 Socket Present State register

The Socket Present State register reflects the current state of the socket. Some of the bits in this register are reflections of interface signals while others are flags set to indicate conditions associated with a status changed event. This register may be written by using the Force Event register.

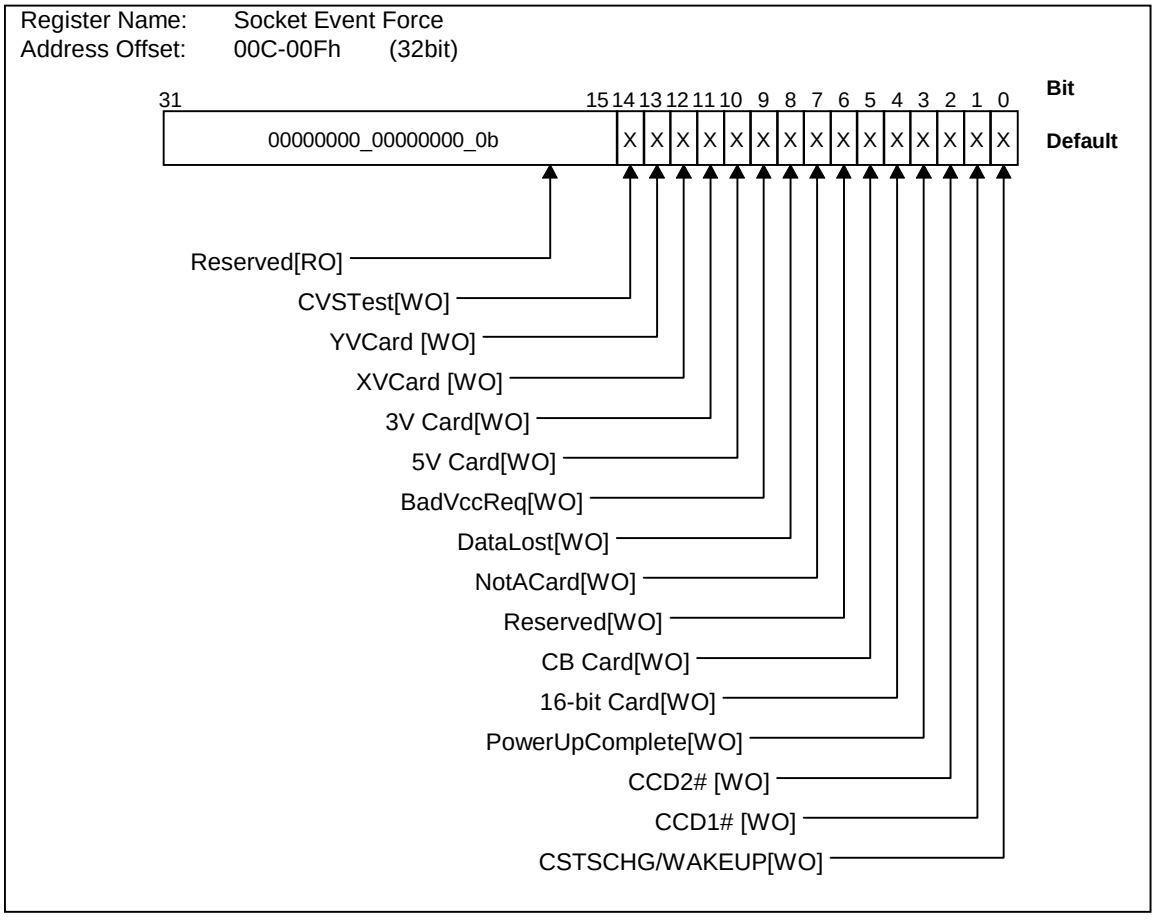


Bit	Field Name	Description
31	YVsocket	When set (1), indicates that the socket can supply Vcc=Y.YV. When cleared (0), indicates that the socket cannot supply Vcc=Y.YV. 5C475 does not support this function. So they always return zero when read.
30	XVsocket	When set (1), indicates that the socket can supply Vcc=X.XV. When cleared (0), indicates that the socket cannot supply Vcc=X.XV. 5C475 does not support this function. So they always return zero when read.
29	3Vsocket	When set (1), indicates that the socket can supply Vcc=3.3V. When cleared (0), indicates that the socket cannot supply Vcc=3.3V. 5C475 supports this function. So they always return one when read.
28	5Vsocket	When set (1), indicates that the socket can supply Vcc=5.0V. When cleared (0), indicates that the socket cannot supply Vcc=5.0V. 5C475 supports this function. So they always return one when read.
27-14	Reserved	This field is reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
13	YVCard	The 5C475 does not support this field. Return zero when read.
12	XVCard	The 5C475 does not support this field. Return zero when read.
11	3VCard	When set (1), indicates that the card inserted will function at Vcc=3.3V. When cleared (0), indicates that the card will not function at Vcc=3.3V. This is determined by interrogating the voltage sense and card detect pins. When a CardBus PC Card is present, and this bit is cleared, the 5C475 must not allow the socket to be powered up at Vcc=3.3V; however, it is possible to be powered up at Vcc=3.3V if 5V Card bit is set to one.
10	5VCard	When set (1), indicates that the card inserted will function at Vcc=5.0V. When cleared (0), indicates that the card will not function at Vcc=5.0V. This is determined by interrogating the voltage sense and card detect pins. When a CardBus PC Card is present, the 5C475 must not allow the socket to be powered up at Vcc=5.0V; however it is possible to be powered up at Vcc=5V when 5V/3.3V Card, although this bit is not set to one.
9	BadVccReq	When set (1), indicates that software attempted to apply a Vcc voltage to a socket that was outside the range detected using the CVS[2::1] and CCD[2::1]# pins.
8	DataLost	When set (1), indicates that a PC card removal event may have caused data to be lost either because a transaction was not completed properly or data was left in the 5C475's buffers. It must be cleared by Card Services when the removal event status changed interrupt is serviced. Writing back a one to this field clears it.
7	NotACard	When set (1), indicates that the type of card inserted could not be determined, the 5C475 does not supply the power to the card. This value does not have to be updated until a recognizable card (e.g. 16-bit PC Card or CardBus PC Card) is inserted.
6	CINT#/IREQ#	When set (1), indicates that the inserted card is driving its interrupt pin true. This bit is not a registered bit and its assertion/deassertion must follow the interrupt pin from the card. This bit reflects the inverted state of CINT#/IREQ# pin as these signals are low true.
5	CBcard	When set (1), indicates that the card inserted was a CardBus PC Card. This value is not updated until a non-CardBus PC Card (e.g. 16-bit PC Card or unrecognized) is inserted. When set, the 5C475 must configure the socket interface for CardBus PC Card.
4	16-bit Card	When set (1), indicates that the card inserted was a 16-bit PC Card. This value is not updated until a non-16-bit PC Card (e.g. CardBus PC Card or unrecognized card) is inserted. When set, the 5C475 configures the socket interface for 16-bit PC Card. Setting this field disables the 5C475's voltage checking hardware so extreme care must be taken when writing the Control register or the hardware could be damaged.
3	PowerCycle	When set (1), indicates that the interface is powered up, i.e. the power up process was successful. When cleared (0), indicates that the interface is powered down, i.e. the power up process was not successful. This field is updated by the 5C475 to communicate the status of each power up/power down request.

Bit	Field Name	Description
2	CCD2#	This field reflects the current state of the CCD2# pin on the interface. 1 indicates CCD2# is High (card is not present), 0 indicates CCD2# is low (card is present). Since the CCD2# pin could be shorted to either CVS1 or CVS2, the value stored here is for when the CVS[2::1] pins are held low.
1	CCD1#	This field reflects the current state of the CCD1# pin on the interface. 1 indicates CCD1# is High (card is not present), 0 indicates CCD1# is low (card is present). Since the CCD1# pin could be shorted to either CVS1 or CVS2, the value stored here is for when the CVS[2::1] pins are held low.
0	CSTSCHG/WAKEUP	This field reflects the current state of the CSTSCHG/WAKEUP# pin on the interface. 1 indicates CSTSCHG/WAKEUP# is asserted, 0 indicates it is deasserted. This bit is meaningless when a 16-bit PC Card is installed. CSTSCHG/WAKEUP# interrupts generated by 16-bit PC Cards are controlled via registers in that interface register space.

6.5.2 Socket Event Force register

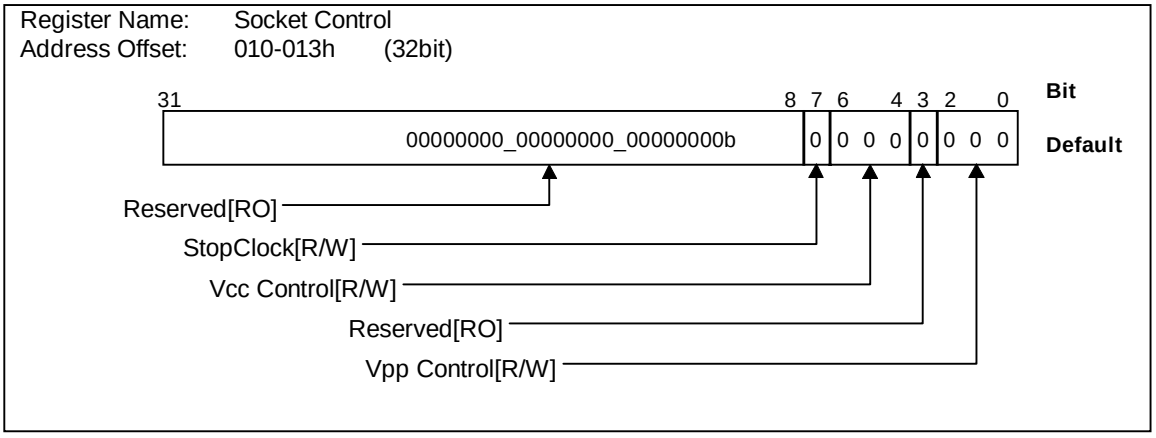
The Socket Event Force register is a phantom register. This register provides software the ability to simulate events by forcing values in the socket's Event and Present State registers. And also, this register provides software the ability to test and restore status. Writing a one to a bit in this register sets the corresponding bit in the socket's Event and Preset State registers.



Bit	Field Name	Description
31-15	Reserved	This field is reserved for future use. Writing to this field has no meaning.
14	CVStest	When written to a 1, causes the 5C475 to interrogate the CVS[2::1] and CCD# pins and update the xVCard fields in the Present State register. This action also re-enables the socket to power up Vcc if the xVCard fields had been previously forced.
13	YVCard	The 5C475 doesn't support this function. Writing to this field has no meaning.
12	XVCard	The 5C475 doesn't support this function. Writing to this field has no meaning.
11	3VCard	Writing to this field cause the 3V Card field in the Present State register to be written. Setting this field disable the socket's ability to power up Vcc until the CVStest field is set. To change the voltage of a card, after forcing this bit, the bridge must either receive a PCIRST# or retest the card's supported voltages. The latter can be accomplished by forcing the CVStest bit. This is necessary to prevent software from applying an incorrect voltage to the 5C475.
10	5VCard	Writing to this field cause the 5V Card field in the Present State register to be written. Setting this field disable the socket's ability to power up Vcc until the CVStest field is set in the Force register. To change the voltage of a card, after forcing this bit, the bridge must either receive a PCIRST# or retest the card's supported voltages. The latter can be accomplished by forcing the CVStest bit. This is necessary to prevent software from applying an incorrect voltage to the 5C475.
9	BadVccReq	Writing to this field cause the BadVccReq field in the Present State register to be written.
8	DataLost	Writing to this field cause the DataLost field in the Present State register to be written.
7	NotACard	Writing to this field cause the NotACard field in the Present State register to be written. If a card is present in the socket (i.e. CCD1# and CCD2# are asserted), writing to this field are ignored.
6	Reserved	This field is reserved for future use. Writing to this field has no meaning.
5	CB Card	Writing to this field cause the CB Card field in the Present State register to be written. If a card is present in the socket (i.e. CCD1# and CCD2# are asserted), writing to this field are ignored.
4	16-bit Card	Writing to this field cause the 16-bit PC Card field in the Present State register to be written. If a card is present in the socket (i.e. CCD1# and CCD2# are asserted), writing to this field are ignored.
3	PowerUpComplete	Writing a 1 to this field simulates the successful completion of a power cycle event by causing the PowerCycle field in the Event register to be set. Note that the PowerCycle field in the Present State register is not affected and continues to reflect the present state of the interface power. Writing a 0 has no meaning.
2	CCD2#	Writing a 1 to this field causes the CCD2# field in the Event register to be set. Note that the CCD2# field in the Present State register is not affected and continues to reflect the present state of the CCD2# pin. Writing a 0 has no meaning.
1	CCD1#	Writing a 1 to this field causes the CCD1# field in the Event register to be set. Note that the CCD1# field in the Present State register is not affected and continues to reflect the present state of the CCD1# pin. Writing a 0 has no meaning.
0	CSTSCHG	Writing a 1 to this field simulates the assertion of the CSTSCHG pin. This results in the Event register's CSTSCHG field being set. Note that the CSTSCHG field in the Present State register is not affected and continues to reflect the present state of the CSTSCHG pin. Writing a 0 has no meaning.

6.5.3 Socket Control register

The Socket Control Register provides control of the socket's Vcc and Vpp. All bits in this register is cleared to zero and the power is removed from the socket when PCITST# is asserted. The supply voltage to the PC card is determined by the interrogation of CCD1#, CCD2#, CVS1, and CVS2 according to the card type detection mechanism described in the CardBus specification. The 5C475 do not supply a Vcc voltage that is not indicated by the VS decode.



Bit	Field Name	Description
31-8	Reserved	This field is reserved for future use. This field is read-only and returns zero when read. Writing to this field has no meaning.
7	StopClock	Setting this bit to one, stops the CardBus clock complying CCLKRUN# protocol. If the card does not support this protocol, the CardBus clock will be stopped regardless of the card status. The default after reset is zero.
6-4	Vcc Control	This field is used to control the Vcc power to the PC Card via external control logic. The bridge determines the voltages that can be applied by decoding the CD and VS signals per the CardBus specification. Those bits and the voltages available in the system determine the correct Vcc options. The value written to this register must agree with the value needed to apply the correct value of Vcc. The bridge must not allow an incorrect Vcc voltage to be applied to a socket. The voltages available are shown in the Status Register. Bit 654 — VCC3EN# — VCC5EN#* 000 Requested Vcc voltage = power off — H — H 001 Reserved — H — H 010 Requested Vcc voltage = 5.0V — L — H 100 Reserved — H — H 101 Reserved — H — H 110 Reserved — H — H 111 Reserved — H — H * if permitted
3	Reserved	This bit is reserved for future use. This bit is read-only and returns zero. Writing to this field has no meaning.
2-0	Vpp Control	This field is used to switch the Vpp power using external Vpp control logic, The bridge has no knowledge of a card's Vpp voltage requirement. Software must determine the needed voltage from the card's CIS. Bit 210 — VPPEN0 — VPPEN1* 000 Requested Vpp voltage = power off — L — L 001 Requested Vpp voltage = 12.0V — L — H 010 Requested Vpp voltage = 5.0V — H — L 011 Requested Vpp voltage = 3.3V — H — L 100 Reserved — L — L 101 Reserved — L — L 110 Reserved — L — L 111 Reserved — L — L * if permitted

7 16-BIT(PC CARD-16) SOCKET STATUS/CONTROL REGISTERS

7.1 Overview

PC Card-16 Socket Status/Control Registers manage status changed events, remote wakeup events, PC Card insertion/removal, and status information about the PC Card in the socket. These registers are used only for PC Card-16.

7.2 Register Space mapping

Socket Status/Control Registers for PC Card-16 are placed in the top 2Kbyte of the memory mapped I/O space of 4Kbyte pointed by the PC Card Control Register Base Address Register and start at offset 800h. (The bottom 2Kbyte are assigned to PC Card-32 Socket Status/Control Registers.) These register can be also accessed through INDEX/DATA port residing I/O address 3E0/3E2, and maintain the backward compatibility with ISA-PCMCIA controllers.

7.3 Register Configuration

Each socket has PC Card-16 Socket Status/Control Registers which consist of 64 BYTE registers. One set of registers are described in the following sections, with the address offset for each socket. Address offset 845h through FFCh are assigned to reserved register. The reserved registers return 00000000h when read. Writing to the reserved registers has no effect.

Mapping Offset	Legacy Index A	Register Name	Mnemonic	Note
800h	00h	Identification and Revision	IDREVS	
801h	01h	Interface Status	IFSTAT	
802h	02h	Power Control	PWCTRL	
803h	03h	Interrupt and General Control	IGCTRL	
804h	04h	Card Status Change	CSCHG	
805h	05h	Card Status Change Interrupt Configuration	CSCINT	
806h	06h	Address Window Enable	AWINEN	
807h	07h	I/O control	IOCTRL	
808h	08h	I/O address 0 Start Low Byte	IOSTL0	
809h	09h	I/O address 0 Start High Byte	IOSTH0	
80Ah	0Ah	I/O address 0 Stop Low Byte	IOSPL0	
80Bh	0Bh	I/O address 0 Stop High Byte	IOSPH0	
80Ch	0Ch	I/O address 1 Start Low Byte	IOSTL1	
80Dh	0Dh	I/O address 1 Start High Byte	IOSTH1	
80Eh	0Eh	I/O address 1 Stop Low Byte	IOSPL1	
80Fh	0Fh	I/O address 1 Stop High Byte	IOSPH1	
810h	10h	System Memory Address 0 Mapping Start Low Byte	SMSTL0	
811h	11h	System Memory Address 0 Mapping Start High Byte	SMSTH0	
812h	12h	System Memory Address 0 Mapping Stop Low Byte	SMSPL0	
813h	13h	System Memory Address 0 Mapping Stop High Byte	SMSPH0	
814h	14h	Card Memory Offset Address 0 Low Byte	MOFFL0	
815h	15h	Card Memory Offset Address 0 High Byte	MOFFH0	
816h	16h	Card Detect and General Control	CDGENC	

Mapping Offset	Legacy Index A	Register Name	Mnemonic	Note
817h	17h	Reserved	RSRVD	
818h	18h	System Memory Address 1 Mapping Start Low Byte	SMSTL1	
819h	19h	System Memory Address 1 Mapping Start High Byte	SMSTH1	
81Ah	1Ah	System Memory Address 1 Mapping Stop Low Byte	SMSPL1	
81Bh	1Bh	System Memory Address 1 Mapping Stop High Byte	SMSPH1	
81Ch	1Ch	Card Memory Offset Address 1 Low Byte	MOFFL1	
81Dh	1Dh	Card Memory Offset Address 1 High Byte	MOFFH1	
81Eh	1Eh	16 bit Global Control	GLCTRL	
81Fh	1Fh	ATA Control	ATCTRL	
820h	20h	System Memory Address 2 Mapping Start Low Byte	SMSTL2	
821h	21h	System Memory Address 2 Mapping Start High Byte	SMSTH2	
822h	22h	System Memory Address 2 Mapping Stop Low Byte	SMSPL2	
823h	23h	System Memory Address 2 Mapping Stop High Byte	SMSPH2	
824h	24h	Card Memory Offset Address 2 Low Byte	MOFFL2	
825h	25h	Card Memory Offset Address 2 High Byte	MOFFH2	
826h	26h	Reserved	RSRVD	
827h	27h	Reserved	RSRVD	
828h	28h	System Memory Address 3 Mapping Start Low Byte	SMSTL3	
829h	29h	System Memory Address 3 Mapping Start High Byte	SMSTH3	
82Ah	2Ah	System Memory Address 3 Mapping Stop Low Byte	SMSPL3	
82Bh	2Bh	System Memory Address 3 Mapping Stop High Byte	SMSPH3	
82Ch	2Ch	Card Memory Offset Address 3 Low Byte	MOFFL3	
82Dh	2Dh	Card Memory Offset Address 3 High Byte	MOFFH3	
82Eh	2Eh	Reserved	RSRVD	
82Fh	2Fh	Misc Control 1	MISCC1	
830h	30h	System Memory Address 4 Mapping Start Low Byte	SMSTL4	
831h	31h	System Memory Address 4 Mapping Start High Byte	SMSTH4	
832h	32h	System Memory Address 4 Mapping Stop Low Byte	SMSPL4	
833h	33h	System Memory Address 4 Mapping Stop High Byte	SMSPH4	
834h	34h	Card Memory Offset Address 4 Low Byte	MOFFL4	
835h	35h	Card Memory Offset Address 4 High Byte	MOFFH4	
836h	36h	Card I/O Offset Address 0 Low Byte	IOFFL0	
837h	37h	Card I/O Offset Address 0 High Byte	IOFFH0	
838h	38h	Card I/O Offset Address 1 Low Byte	IOFFL1	
839h	39h	Card I/O Offset Address 1 High Byte	IOFFH1	
83Ah	3Ah	General Purpose I/O	GPIO	
83Bh	3Bh	Reserved	RSRVD	
83Ch	3Ch	Reserved	RSRVD	
83Dh	3Dh	Reserved	RSRVD	
83Eh	3Eh	Reserved	RSRVD	
83Fh	3Fh	Reserved	RSRVD	
840h	NA	System Memory Page Address 0	SMPGA0	
841h	NA	System Memory Page Address 1	SMPGA1	
842h	NA	System Memory Page Address 2	SMPGA2	

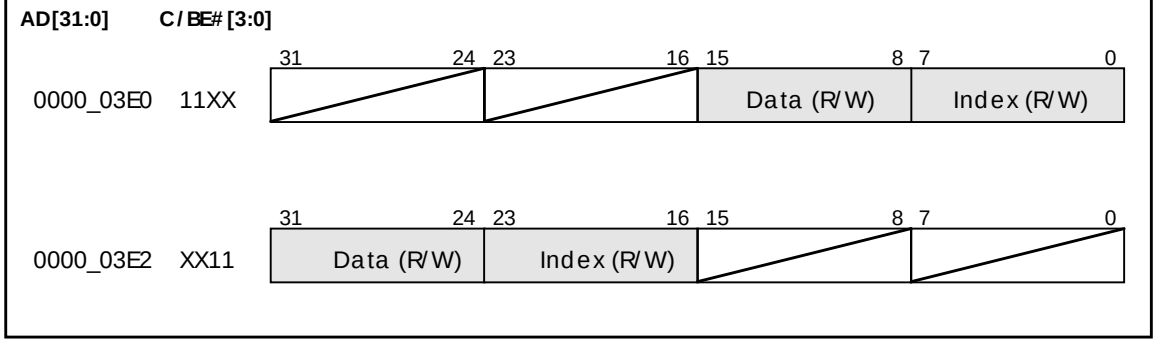
Mapping Offset	Legacy Index A	Register Name	Mnemonic	Note
843h	NA	System Memory Page Address 3	SMPGA3	
844h	NA	System Memory Page Address 4	SMPGA4	

7.4 PCIC Compatible mode (Legacy Mode)

The 5C475 support the PCIC compatible mode, i.e. Legacy mode, that all 16-bit Card Sockets Status/Control registers can be accessed through INDEX/DATA ports which is located at I/O address 03E0h or 03E2h. PCIC compatible mode is enabled by writing a non-zero address to 16-bit Legacy Mode Base Address register. The index register and data register are contiguous in the I/O address space so that a single 16-bit instruction can simultaneously write to the index and data registers. The index range can be set to either 00h to 3Fh or 80h to BFh for the socket A by setting the Index Range Select bit (bit3) in the 16-bit Interface Control register in the PCI configuration space.

The below figure shows the status of INDEX/DATA ports when the Legacy Base Address register is set to 03E0h or 03E2h.

Register Name: Legacy Index/Data Port
PCI I/O Address : 03E0h (or 03E2h)

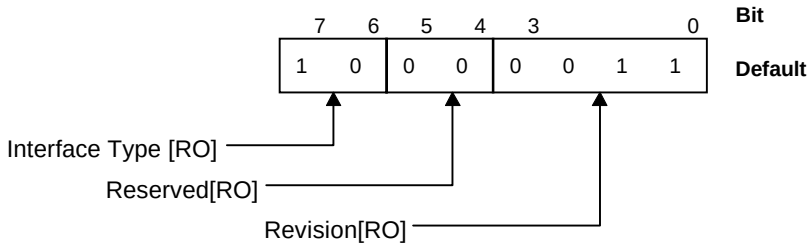


7.5 General Setup Registers

7.5.1 Identification and Revision register

This register provides the software with information on PC Card-16.

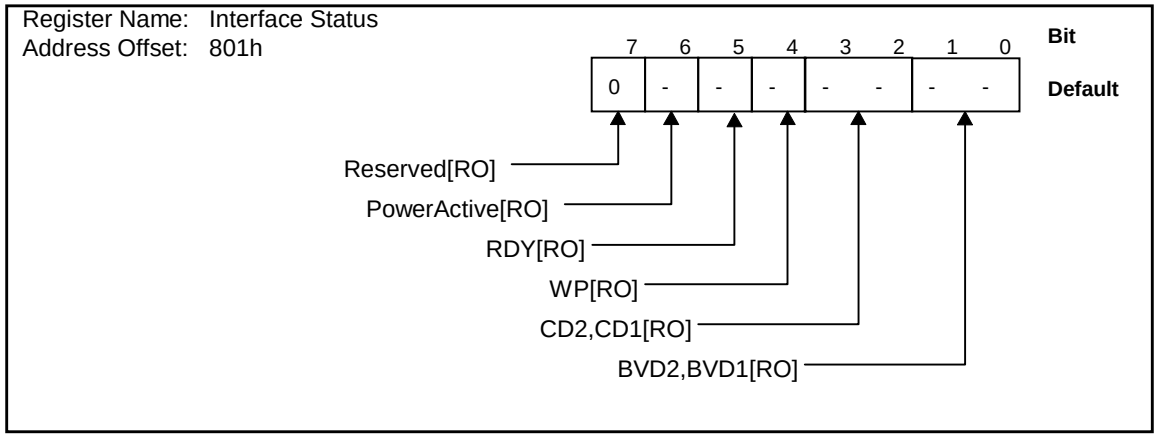
Register Name: Identification and Revision
Address Offset: 800h



Bit	Field Name	Description
7-6	InterfaceType	This field indicates the type of PC Card-16 supported by the 5C475. The 5C475 supports the 16-bit card on the Memory and I/O interface and return 10b when read. 00 I/O only 01 Memory 10 Memory & I/O 11 Reserved
5-4	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read.
3-0	Revision	This field indicates PCIC revision number. This filed is read-only and returns 0011b when read.

7.5.2 Interface Status register

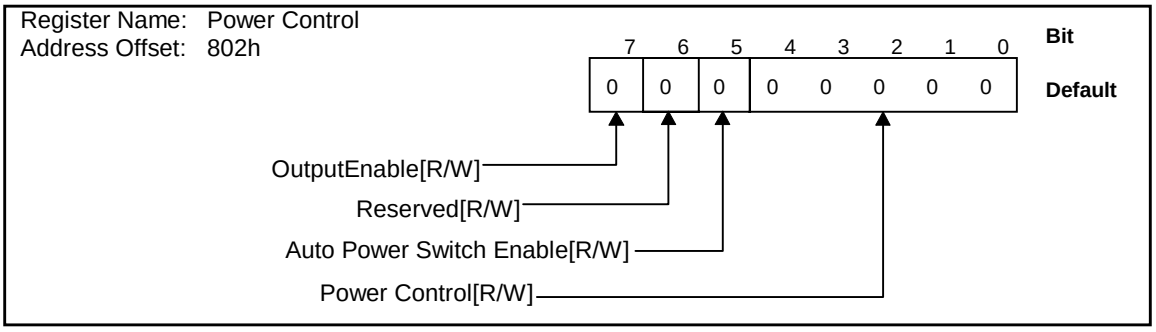
This register provides information on the status of the PC Card interface.



Bit	Field Name	Description
7	Reserved	This bit is reserved for future use. This bit is read-only and returns zero when read. Writing to this field has no effect.
6	PowerActive	This bit indicates whether or not the socket power is on (3.3V or 5V). This bit is set to one when either VCC3EN# or VCC5EN# is turned on, and set to zero when the socket power is turned off.
5	RDY	This bit indicates the state of the READY/IREQ# input signal. This bit is available only on the PC Card-16 memory interface, and has no meaning on the I/O interface. 0 : memory card is busy. 1 : memory card is ready.
4	WP	This bit indicates the state of the WP/IOIS16# input signal. The memory card will not be write protected unless the WriteProtect bit in the Card Memory Offset High Byte register is set to one, even if the WP signal is a one to maintain the compatibility with 82365SL B-Step. This bit is available only on the PC Card-16 memory interface.
3-2	CD2,CD1	This field returns the inverse state of CD2# and CD1# when read.
1-0	BVD2,BVD1	These bits have meanings which depend on the type of the PC Card-16 inserted in the socket. When a 16-bit memory card is inserted, this field indicates the state of the battery voltage detect signals (BVD1,BVD2) as follows: BVD2 BVD1 bit1 bit0 Card Battery Low Low 0 0 Battery Dead Low High 0 1 Warning High Low 1 0 Battery Dead High High 1 1 Battery Good When a 16-bit I/O card is inserted, Bit 0 in this field indicates the state of the BVD1#/STSCHG#/RI# input signal when the Ring Indicate Enable bit in the Interrupt and General Control register is a zero.

7.5.3 Power Control register

This register controls the output of the 5C475 to the PC Card-16 socket. This register can also control the socket power to maintain the compatibility with the PCIC.



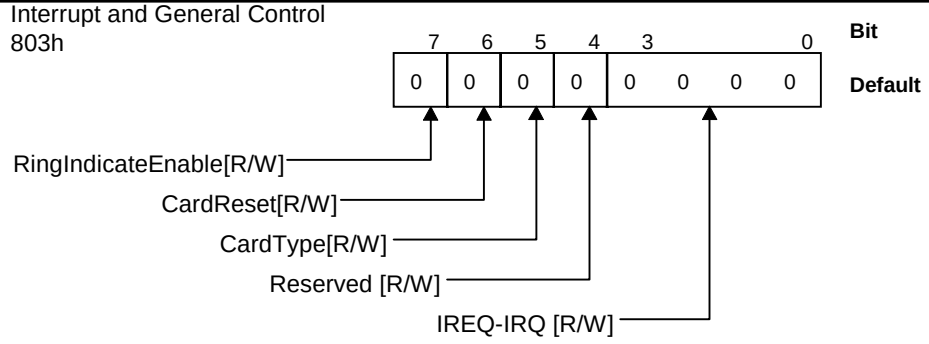
Bit	Field Name	Description
7	OutputEnable	When the 5C475 is on the 16-bit card mode, the output signals listed below are tri-stated when this bit is set to zero, and they are not tri-stated when this bit is set to one. The following output signals are the object : CE1#, CE0#,IORD#,IOWR#, OE#, WE#, RESET, ADR[25:0], DATA[15:0], REG#
6	Reserved(R/W)	This read/write bit is reserved for future use. Writing to this bit has no effect. The default after reset is zero.
5	Auto Power Switch Enable	When this bit is set to one, the automatic socket power switching based on the card detection is enabled.
4-0	Power Control	This bit field is used with Bit 0 in the Misc Control 1 register to control VCC3EN#,VCC5EN#,VPPEN0 and VPPEN1. Writing to these bits is enabled only when the power is on or the voltage is changed. The following table shows the relation between power control signals and this bit field.

Bit4	Bit3	Bit2	Bit1	Bit0	Misc Control 1 Bit0	VCC3EN#	VCC5EN#	VPPEN1	VPPEN0
1	X	X	0	0	0	1	0	0	0
1	X	X	0	0	1	0	1	0	0
1	X	X	0	1	0	1	0	0	1
1	X	X	0	1	1	0	1	0	1
1	X	X	1	0	0	1	0	1	0
1	X	X	1	0	1	0	1	1	0
1	X	X	1	1	0	1	0	1	1
1	X	X	1	1	1	0	1	1	1
0	X	X	X	X	X	1	1	0	0

7.5.4 Interrupt and General Control register

This register controls Ring Indicate Enable, Card Reset, Card Type and Interrupt Steering of IRQs from I/O PC Card-16.

Register Name: Interrupt and General Control
Address Offset: 803h



Bit	Field Name	Description
7	RingIndicateEnable	On the I/O card interface mode, when this bit is set to one, the STSCHG#/RI# from the PC Card-16 signal is used as a Ring Indicator signal and is passed through to the RI_OUT# pin and when this bit is set to zero, the STSCHG#/RI# from the I/O PC Card-16 signal is used as the status change signal STSCHG#. The current status of the signal is then available to the read from the Interface Status register and this signal can be configured as a source for the card status change interrupt. This bit has no meaning on the memory card interface mode.
6	CardReset	When this bit is set to zero, the Reset signal to the PC Card-16 is activates. This signal will be active until this bit is set to one,
5	CardType	This bit indicates the PC Card type. When this bit is set to zero, a memory card interface is selected. When this bit is set to one, an I/O card interface is selected.
4	Reserved(R/W)	This read/write bit is reserved for future use.
3-0	IREQ-IRQ	This field selects the interrupt routing for the IREQ#/CINT# signal from I/O PC Card-16. These bits are available only when the IREQ-ISA Enable bit in the Bridge control register is set bit3 bit2 bit1 bit0 IRQ selection 0 0 0 0 IRQ disabled 0 0 0 1 Reserved 0 0 1 0 Reserved 0 0 1 1 IRQ3 0 1 0 0 IRQ4 0 1 0 1 IRQ5 0 1 1 0 Reserved 0 1 1 1 IRQ7 1 0 0 0 Reserved 1 0 0 1 IRQ9 1 0 1 0 IRQ10 1 0 1 1 IRQ11 1 1 0 0 IRQ12 1 1 0 1 Reserved 1 1 1 0 IRQ14 1 1 1 1 IRQ15

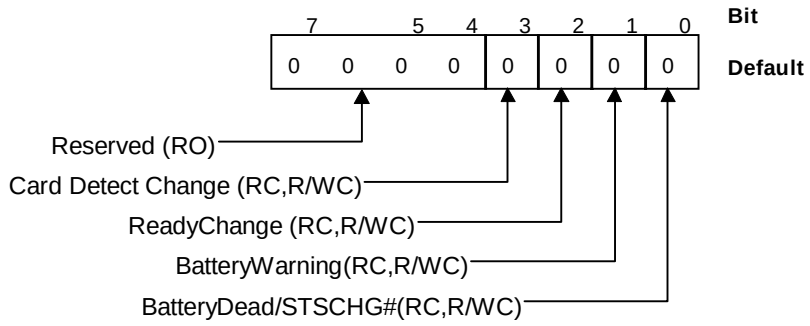
7.5.5 Card Status Change register

This register contains the status for sources of the card status change interrupts. These sources can be enabled to generate a card status change interrupt by setting the corresponding bit in the Card Status Change Interrupt Configuration register. Each bits in this register read back 0 when the corresponding status enable bits in the Card Status change Interrupt Configuration are set to 0.

When the Card Status Change Acknowledge mode bit in the 16-bit Global Control register is set to 1, the acknowledgment of sources for the Card Status Change Interrupt is performed by writing back 1 to the appropriate bit in the Cad Status Change Register that was read as 1b. Once the internal source is acknowledged by writing a 1 to the bit, the bit reads back as 0. The interrupt signal INTA# or IRQx responding to the card status change maintains to be active, if enabled on a system IRQ line, until all of the bits in this register are zero. When the Card Status Change Acknowledge mode bit in the 16-bit Global Control register is not set, the Card Status Change Interrupt signal maintains to be active, if enabled on a system IRQ line, until the Card Status Change register is read. The read operation to the Card Status Change register resets all bits in the register.

If two or more Card Status Change Interrupt are pending or a Card Status Change Interrupt condition occurs while another is being serviced, the 5C475 does not generate a second interrupt. The interrupt service routing must read the Card Status Change register to ensure that all interrupt requests are serviced before exiting the service routines.

Register Name: Card Status Change
Address Offset: 804h

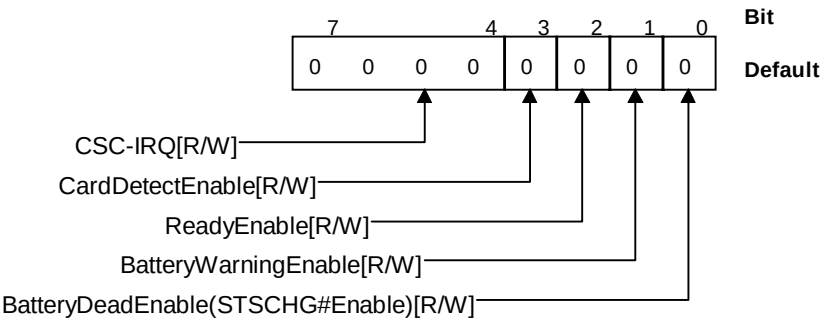


Bit	Field Name	Description
7-4	Reserved	This field is reserved for future use. This field is read-only and returns zeros when read.
3	Card Detect Change	This bit is set to 1 when a change on either CD1# or CD2# signals occurs. This bit is not set unless the Card Detect Enable bit in the Card Status Change Interrupt Configuration register is set. Both CCD1# and CCD2# bits in the Socket Event register are cleared by a read clear or a write back clear. And also, this bit is cleared when either CCD1# or CCD2#, or both of CCD1# and CCD2# are cleared by a write back clear.
2	ReadyChange	This bit is set to1 when a low-to-high transition occurs on the RDY/BSY# signal, indicating that the memory PC Card-16 is ready to accept a new data transfer. This bit is not set unless the Ready Enable bit in the Card Status Change Interrupt Configuration register is set. This bit is always zero on I/O PC Card-16.
1	BatteryWarning	This bit is set to1 when a battery warning condition is detected. This bit is not set unless the Battery Warning Enable bit in the Card Status Change Interrupt Configuration register is set. This bit is always zero on I/O PC Card-16.
0	BatteryDead /STSCHG#	On the memory PC Card-16 interface mode, this bit is set to 1 when a battery dead condition is detected. On the I/O PC Card-16 interface mode, this bit is set to 1 when the BVD1/STSCHG# signal is asserted “low”, but then, this bit reads back as 0 if the Ring Indicate Enable bit in the Interrupt and General Control register is set to 1. This bit is not set unless the Battery Enable bit in the Card Status Change Interrupt Configuration register is set.

7.5.6 Card Status Change Interrupt Configuration register

This register controls the steering of Card Status Change Interrupt and the enabling of Card Status Change Interrupt.

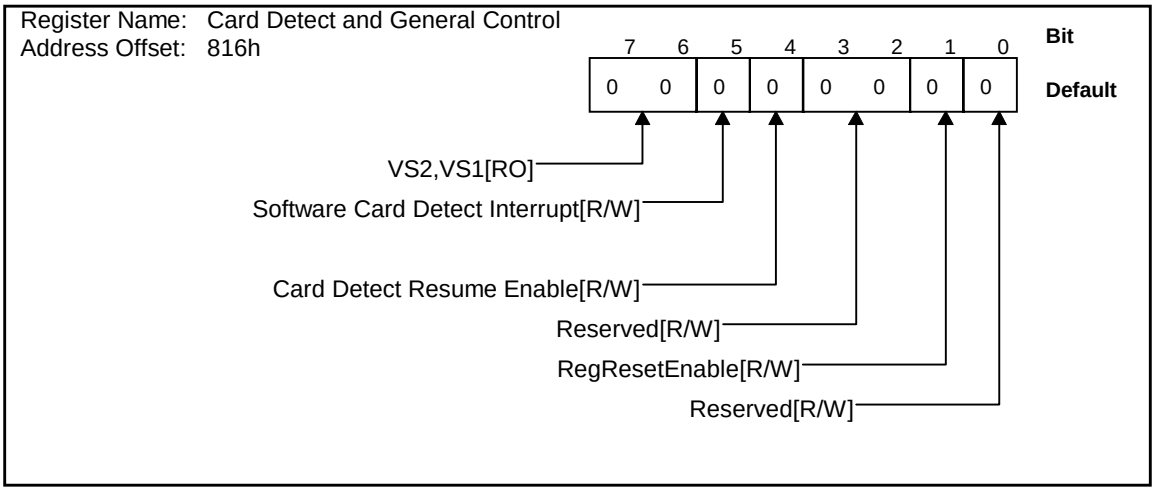
Register Name: Card Status Change InterruptConfiguration
Address Offset: 805h



Bit	Field Name	Description
7-4	CSC-IRQ	This field selects the interrupt routing for card status change interrupts. When this field is set to the reserved value or 0000b, the card status change interrupt is routed to INTA#. The default after reset is 0000b. This field is reset when the RegResetEnable bit in the Card Detect and General Control register is set and the card is removed. bit7 bit6 bit5 bit4 IRQ selection 0 0 0 0 IRQ disabled 0 0 0 1 Reserved 0 0 1 0 Reserved 0 0 1 1 IRQ3 0 1 0 0 IRQ4 0 1 0 1 IRQ5 0 1 1 0 Reserved 0 1 1 1 IRQ7 1 0 0 0 Reserved 1 0 0 1 IRQ9 1 0 1 0 IRQ10 1 0 1 1 IRQ11 1 1 0 0 IRQ12 1 1 0 1 Reserved 1 1 1 0 IRQ14 1 1 1 1 IRQ15
3	CardDetectEnable	When this bit is set to 1, the interrupt is generated when a change is detected on either CD1# or CD2#.
2	ReadyEnable	Setting this bit to 1 enables the card status change interrupt when a low-to-high transaction occurs on the RDY/BSY# signal. This bit has no meaning on the I/O PC Card-16 interface.
1	BatteryWarningEnable	Setting this bit to 1 enables the card status change interrupt when a battery warning conditions is detected. This bit has no meaning on the I/O PC-Card-16 interface.
0	BatteryDeadEnable (STSCHG#Enable)	Setting this bit to 1 enables a Card Status Change Interrupt when a battery dead condition is detected in a memory PC Card-16. In an I/O PC Card-16, setting this bit to 1 enables a Card Status Change Interrupt when the BVD1/STSCHG# signal is pulled “Low”. Setting this bit to 0 disables the interrupt.

7.5.7 Card Detect and General Control register

This register is used to reset the configuration registers and report the selected status of voltage stored to the card.

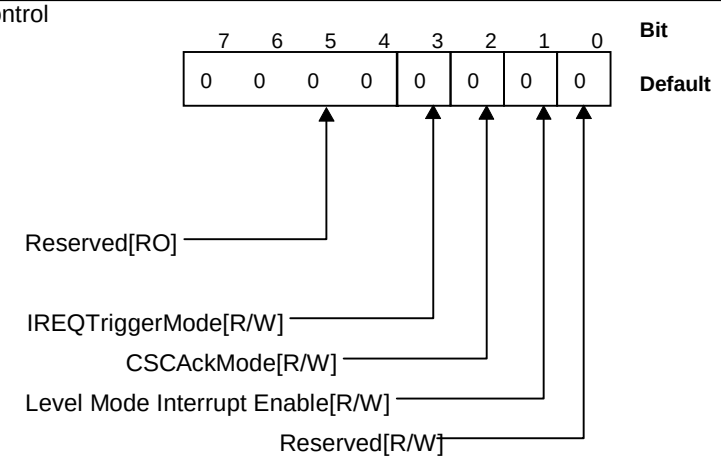


Bit	Field Name	Description
7-6	VS2,VS1	These bits indicate the state of VS2 and VS1. The default after reset is zero.
5	Software Card Detect Interrupt	Setting this bit to 1 enables to generate the Card Detected Interrupt, and then one should note that both CCD1# and CCD2# bits in the Socket Event register are set by writing to this bit. This bit is a phantom bit and returns zero when read.
4	Card Detect Resume Enable	When this bit is set to1, then once a card detect change is detected on the CD1# or CD2# inputs, RI_OUT# output goes from “high” to “low”.
3-2	Reserved	This read/write field is reserved for future use. The default after reset is zero.
1	RegResetEnable	When this bit is set to 1, a reset pulse is generated to reset the following configuration registers for the socket to their default state (zero’s) when both the CD1# and CD2# inputs for the socket go “high”. Interrupt and General Control Card Status Change Interrupt Configuration (CSC-IRQ bits only*) Address Window Enable I/O Control I/O Address {0,1} Start Low Byte I/O Address {0,1} Start High Byte I/O Address {0,1} Stop Low Byte I/O Address {0,1} Stop High Byte System Memory Address {0,1,2,3,4} Start Low Byte System Memory Address {0,1,2,3,4} Start High Byte System Memory Address {0,1,2,3,4} Stop Low Byte System Memory Address {0,1,2,3,4} Stop High Byte Card Memory Offset Address {0,1,2,3,4} Start Low Byte Card Memory Offset Address {0,1,2,3,4} Start High Byte Card Memory Offset Address {0,1,2,3,4} Stop Low Byte Card Memory Offset Address {0,1,2,3,4} Stop High Byte
0	Reserved	This read/write bit is reserved for future use. The default after reset is zero.

7.5.8 16 bit Global Control register

This register controls both PC Card sockets, and is not duplicated for each socket. PCI reset clears all bits in this register.

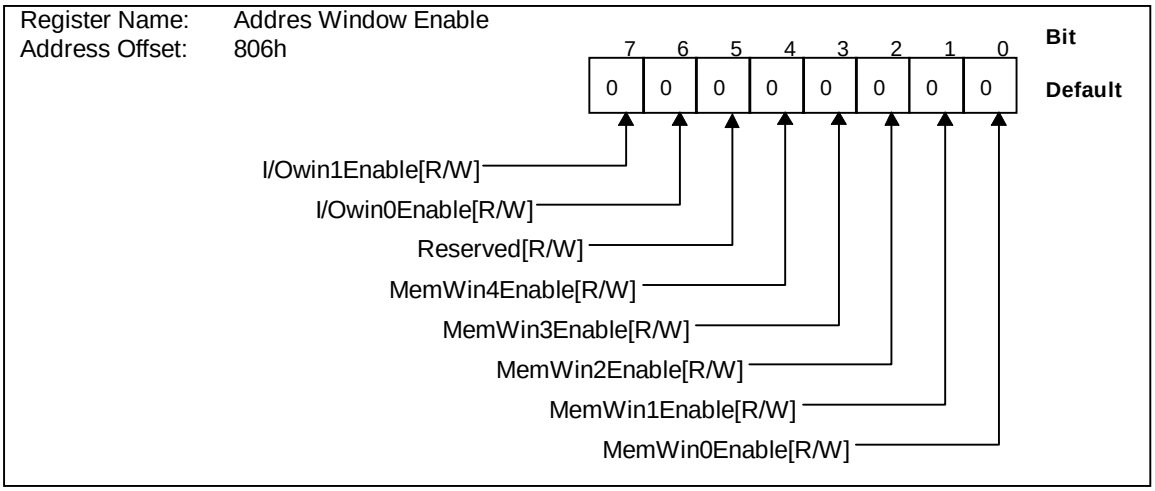
Register Name: 16 bit Global Control
Address Offset: 81Eh



Bit	Field Name	Description
7-4	Reserved	This field is reserved for future use. This field is read-only and returns zero when read.
3	IREQTriggerMode	This bit selects level mode interrupts for IRQx generated by the particular PC card interrupts. When this bit is set to 1, it selects level mode. And also when this bit is set to 0, it selects edge mode. The default is zero.
2	CSCAckMode	When this bit is set to 1, each Card Status Change Interrupt is acknowledged with an explicit write of 1 to the Card Status Change register bit that identifies the interrupt. - a corresponding bit is reset to 0. When this bit to 0, each Card Status Change Interrupt is acknowledged by reading the Card Status Change register. - all bits are reset to 0.
1	Level Mode Interrupt Enable	When this bit is set to1, level mode is selected. And IRQx go from tri-stated to low whenever the interrupt is active. When this bit is set to 0, edge mode is selected. And IRQx go from tri-stated to low when the interrupt is enabled, and go from low to high when the interrupt is active, and also go to low when the interrupt is inactive. This bit is tri-stated when the interrupt is disabled.
0	Reserved(R/W)	This read/write bit is reserved for future use.

7.5.9 Address Window Enable register

This register controls enabling of the memory and I/O mapping windows to the PC Card memory or I/O space. All bits in this register are cleared after reset.

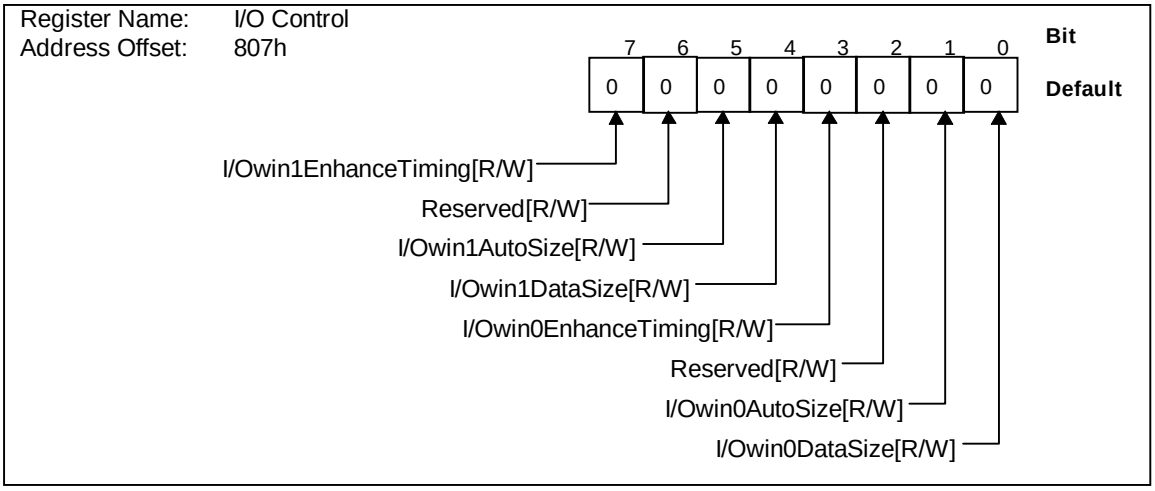


Bit	Field Name	Description
7	I/Owin1Enable	This bit controls whether or not the I/O window 1 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the I/O window 1. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the I/O window 1. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
6	I/Owin0Enable	This bit controls whether or not the I/O window 0 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the I/O window 0. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the I/O window 0. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
5	Reserved(R/W)	This read/write bit is reserved for future use. The default after reset is zero.
4	MemWin4Enable	This bit controls whether or not the memory window 4 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the memory window 4. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the memory window 4. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
3	MemWin3Enable	This bit controls whether or not the memory window 3 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the memory window 3. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the memory window 4. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
2	MemWin2Enable	This bit controls whether or not the memory window 2 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the memory window 2. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the memory window 4. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
1	MemWin1Enable	This bit controls whether or not the memory window 1 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the memory window 1. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the memory window 4. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
0	MemWin0Enable	This bit controls whether or not the memory window 0 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the memory window 0. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the memory window 4. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.

7.6 I/O Window Control Register Description

7.6.1 I/O Control register

This register controls the I/O data path size and the access timing specification for the I/O windows 0 and 1. All bits in this register are cleared after reset.

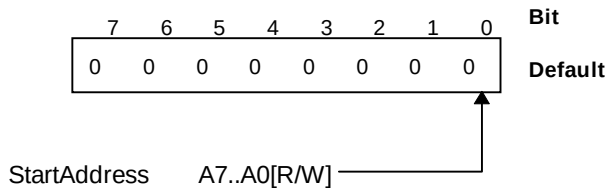


Bit	Field Name	Description
7	I/Owin1EnhanceTiming	When this bit is set to 1, 16-bit I/O card access timing for I/O window 1 is determined by user defined timing in the 16-bit I/O timing 0 register. When this bit is set to 0, the default timing is selected. The default after reset is zero. User defined timing is valid when 16-bit I/O Enhance Timing bit in the 16-bit Interface Control register is set to 1 regardless of this bit being set to 0.
6	Reserved(R/W)	This read/write bit is reserved for future use. The default after reset is zero.
5	I/Owin1AutoSize	This bit indicates how to select the I/O data path size to the PC Card-16. When this bit is set to 1, the data path size for I/O window 1 is determined by the IOIS16# signal from PC Card-16. When this bit is set to 0, it is determined by the I/Owin1DataSize bit.
4	I/Owin1DataSize	This bit selects the I/O data path size to the PC Card-16. When this bit is set to 1, 16-bit data path is selected. When this bit is set to 0, 8-bit data path is selected. This bit is ignored when I/Owin1AutoSize is 1b. This bit takes precedence of PCI command.
3	I/Owin0EnhanceTiming	When this bit is set to 1, 16-bit I/O card access timing for I/O window 0 is determined by user defined timing in the 16-bit I/O timing 0 register. when this bit is set to 0, the default timing is selected. The default after reset is zero. User defined timing is valid when 16-bit I/O Enhance Timing bit in the 16-bit Interface Control register is set to 1 regardless of this bit being set to 0.
2	Reserved(R/W)	This read/write bit is reserved for future use. The default after reset is zero.
1	I/Owin0AutoSize	This bit indicates how to select the I/O data path size to the PC Card-16. When this bit is set to 1, the data path size for I/O window 0 is determined by the IOIS16# signal from PC Card-16. When this bit is set to 0, it is determined by the I/Owin0DataSize bit.
0	I/Owin0DataSize	This bit selects the I/O data path size to the PC Card-16. When this bit is set to 1, 16-bit data path is selected. When this bit is set to 0, 8-bit data path is selected. This bit is ignored when I/Owin0AutoSize is 1b. This bit has priority over the PCI command.

7.6.2 I/O Address 0-1 Start Low Byte register

These two registers contain the lower address bits that are used to determine the start address of the corresponding I/O address windows 0 and 1. This provides a minimum 1 byte window for the corresponding I/O address window if the start address and stop address are the same.

Register Name: I/O Address 0-1 Start Low Byte
Address Offset: 808h,80Ch



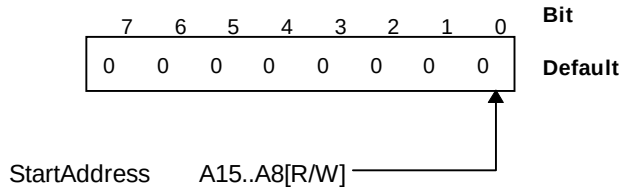
	Window 0	*Window 1*
Offset	808h	80Ch

Bit	Field Name	Description
7-0	StartAddress A7..A0	I/O Window 0-1 Start Address A7 .. A0:

7.6.3 I/O Address 0-1 Start High Byte register

These two registers contain the upper address bits that are used to determine the start address of the corresponding I/O address windows 0 and 1.

Register Name: I/O Address 0-1 Start High Byte
Address Offset: 809h,80Dh



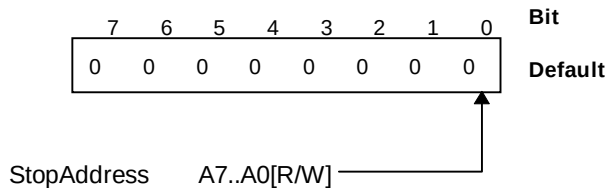
	Window 0	*Window 1*
Offset	809h	80Dh

Bit	Field Name	Description
7-0	StartAddress A15..A8	I/O Window 0-1 Start Address A15..A8:

7.6.4 I/O Address 0-1 Stop Low Byte register

These two registers contain the lower address bits that are used to determine the top address of the corresponding I/O address windows 0 and 1. This provides a minimum 1 byte window for the corresponding I/O address window if the start address and stop address are the same.

Register Name: I/O Address 0-1 Stop Low Byte
Address Offset: 80Ah,80Eh



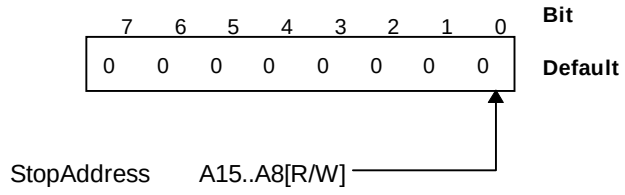
	Window 0	*Window 1*
Offset	80Ah	80Eh

Bit	Field Name	Description
7-0	StopAddress A7..A0	I/O Window 0-1 Stop Address A7 .. A0:

7.6.5 I/O Address 0-1 Stop High Byte register

These two register contain the upper address bits that are used to determine the stop address of the corresponding I/O address windows 0 and 1.

Register Name: I/O Address 0-1 Stop High Byte
Address Offset: 80Bh,80Fh



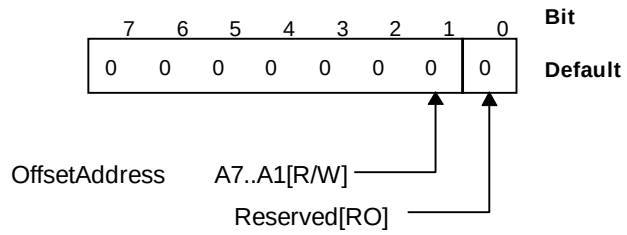
	Window 0	*Window 1*
Offset	80Bh	80Fh

Bit	Field Name	Description
7-0	StopAddress A15..A8	I/O Window 0-1 Stop Address A15..A8:

7.6.6 Card I/O Offset Address 0-1 Low Byte register

These two registers contain the lower offset address bits that are added to system address bits A[7:1] to generate the PC Card-16 I/O address for I/O address windows 0 and 1.

Register Name: Card I/O Offset Address 0-1 Low Byte
Address Offset: 836h,838h



	Window 0	*Window 1*
Offset	836h	838h

Bit	Field Name	Description
7-1	Offset Address A7..A1	I/O Window 0-1 Card I/O Offset Address A7..A1:
0	Reserved	This bit is reserved and returns zero when read.

7.6.7 Card I/O Offset Address 0-1 High Byte register

These two registers contain the upper offset address bits that are added to the system address bits A[15:8] to generate the PC Card-16 I/O address for I/O address windows 0 and 1.

Register Name: Card I/O Offset Address 0-1 High Byte
Address Offset: 837h,839h

	Window 0	*Window 1*
Offset	837h	839h

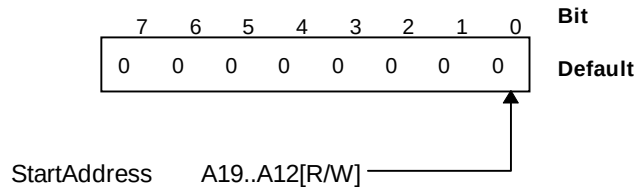
Bit	Field Name	Description
7-0	OffsetAddress A15..A8	I/O Window 0-1Offset Address A15..A8:

7.7 Memory Window Control Registers

7.7.1 System Memory Address 0-4 Mapping Start Low Byte register

These five registers contain the lower address bits that indicate the start address of the system memory address mapping windows 0,1,2,3 and 4. The register's contents correspond to PCI memory address bits A[19:12], and are used to determine whether memory access are valid. Therefore mapping of each system memory can start and stop on any 4Kbyte boundary of the system memory.

Register Name: System Memory Address 0-4 Mapping Start Low Byte
Address Offset: 810h,818h,820h,828h,830h



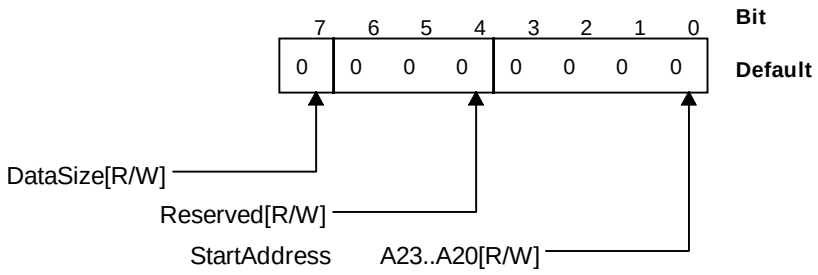
	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	810h	818h	820h	828h	830h

Bit	Field Name	Description
7-0	StartAddress A19..A12	System Memory Address Mapping Window 0-4 Start Address A19 .. A12:

7.7.2 System Memory Address 0-4 Mapping Start High Byte register

These five registers contain the upper address bits that indicate the start address of the system memory address mapping windows 0,1,2,3 and 4. The register's contents correspond to PCI memory address bits A[23:20], and are used to determine whether memory access are valid. And also the data path size of each window is controlled by a bit in its corresponding register.

Register Name: System Memory Address 0-4 Mapping Start High Byte
Address Offset: 811h,819h,821h,829h,831h



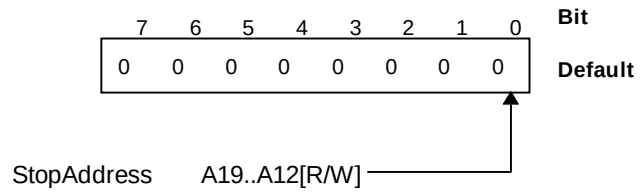
	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	811h	819h	821h	829h	831h

Bit	Field Name	Description
7	DataSize	This bit selects the memory data path size to the PC Card-16. When this bit is set to 1, 16-bit data path is selected. When this bit is set to 0, 8-bit data path is selected. This bit has priority over the PCI command.
6-4	Reserved(R/W)	This read/write bit field is reserved.
3-0	StartAddress A23..A20	System Memory Address Mapping Window 0-4 Start Address A23 .. A20:

7.7.3 System Memory Address 0-4 Mapping Stop Low Byte register

These five registers contain the lower address bits that indicate the stop address of the corresponding system memory address mapping windows 0,1,2,3 and 4. The register's contents correspond to PCI memory address bits A[19:12], and are used to determine whether memory access are valid.

Register Name: System Memory Address 0-4 Mapping Stop Low Byte
Address Offset: 812h,81Ah,822h,82Ah,832h



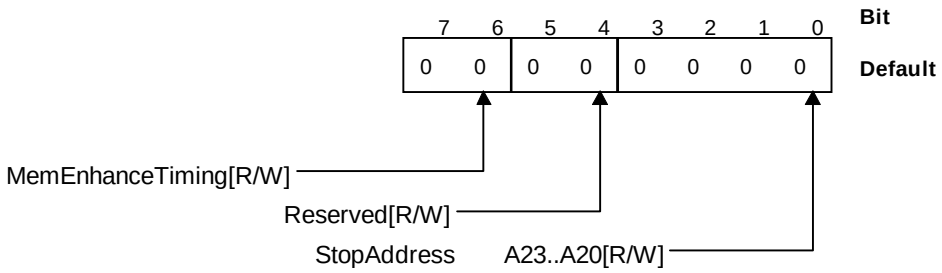
	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	812h	81Ah	822h	82Ah	832h

Bit	Field Name	Description
7-0	StopAddress A19..A12	System Memory Address Mapping Window 0-4 Stopt Address A19 .. A12:

7.7.4 System Memory Address 0-4 Mapping Stop High Byte register

These five registers contain the upper address bits that indicate the stop address of the corresponding system memory address mapping windows 0,1,2,3 and 4. The register's contents correspond to PCI memory address bits A[23:20], and are used to determine whether memory access are valid. Two bits in each of the registers select the PC Card-16 access timing for the corresponding system memory window.

Register Name: System Memory Address 0-4 Mapping Stop High Byte
Address Offset: 813h,81Bh,823h,82Bh,833h



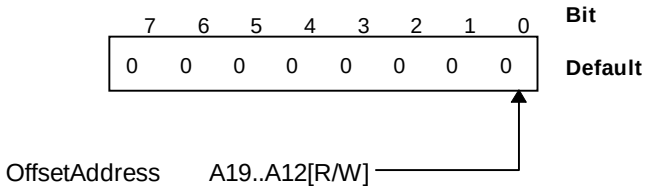
	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	813h	81Bh	823h	82Bh	833h

Bit	Field Name	Description
7-6	MemEnhanceTiming	Timing parameters for memory PC Card-16 are independently configured for each Common Memory Window by programming these timing bits. The default timing mode is 00b, and only the default timing is used for Attribute memory. User defined timing is valid when 16-bit Memory Enhance Timing bit in the 16-bit Interface Control register is set to 1 regardless of this bit being set to 0. 00b = Default Timing 01b = Enhance Timing 10b = Enhance Timing 11b = Enhance Timing
5-4	Reserved(R/W)	This read/write bit field is reserved.
3-0	StopAddress A23..A20	System Memory Address Mapping Window 0-4 Stop Address A23 .. A20:

7.7.5 Card Memory Offset Address 0-4 Low Byte register

These five registers contain the lower offset address bits that are added to system address bits A[19:12] to generate the PC Card-16 memory address for I/O windows 0,1,2,3 and 4.

Register Name: Card Memory Offset Address 0-4 Low Byte
Address Offset: 814h,81Ch,824h,82Ch,834h



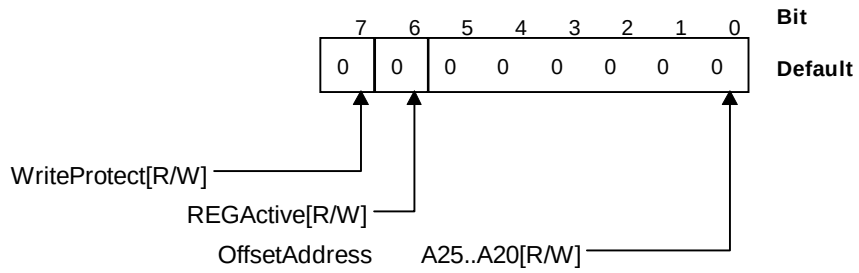
	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	814h	81Ch	824h	82Ch	834h

Bit	Field Name	Description
7-0	OffsetAddress A19..A12	Card Memory Offset Address A19 .. A12:

7.7.6 Card Memory Offset Address 0-4 High Byte register

These five registers contain the upper offset address bits that are added to system address bits A[23:20] to generate the PC Card-16 memory address for I/O windows 0,1,2,3 and 4. These register also control PC Card-16 memory software write protect for the corresponding system memory windows, and select whether the memory windows are mapped to attribute memory, or to common memory on the PC Card-16.

Register Name: Card Memory Offset Address 0-4 High Byte
Address Offset: 815h,81Dh,825h,82Dh,835h (8 bit)



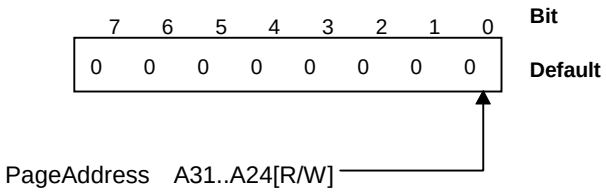
	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	815h	81Dh	825h	82Dh	835h

Bit	Field Name	Description
7	WriteProtect(WP)	When this bit is set to 1, write transactions to the PC Card-16 through the corresponding system memory window are inhibited. When this bit is set to 0, write transactions are allowed. The WP switch on the memory card sets the Memory Write Protect bit in the Interface Status register, but the memory write cycles can be blocked by setting it.
6	REGActive	When this bit is set to 1, accesses to the system memory window are changed over accesses to the attribute memory on the PC Card by asserting REG# “low”. When this bit is set to 0, accesses to the system memory window are changed over accesses to the common memory on the PC Card by asserting REG# “high”.
5-0	OffsetAddress A25..A20	Card Memory Offset Address A25 .. A20:

7.7.7 System Memory Page Address 0-4 register

This register contains an 8 bit page address that allows selection of a 16 Mbyte window page in the 4 Gbyte memory address space in which socket memory window are mapped. Access to a window is allowed only when the page address in the corresponding Card Memory Page Address register matches PCI memory address bits A[31:24], indicating a page hit. Reset clears all bits in this register, so that the default page is the first page (i.e., 0-16 Mbyte address range). This register can not be accessed through I/O address 3E0h/3E2h ports.

Register Name: System Memory Page Address 0-4
Address Offset: 840, 841, 842, 843, 844h (8bit)



	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	840h	841h	842h	843h	844h

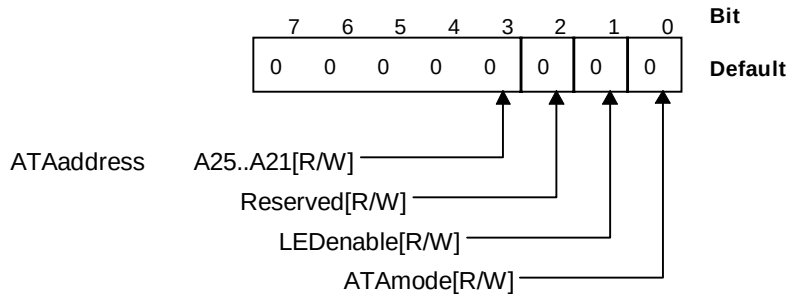
Bit	Field Name	Description
7-0	PageAddress A31..A24	System Memory Page Address A31 .. A24:

7.8 Special Function Registers

7.8.1 ATA Control register

This register contains the information which is used for PCMCIA-ATA mode.

Register Name: ATA Control
Address Offset: 81Fh (8 bit)

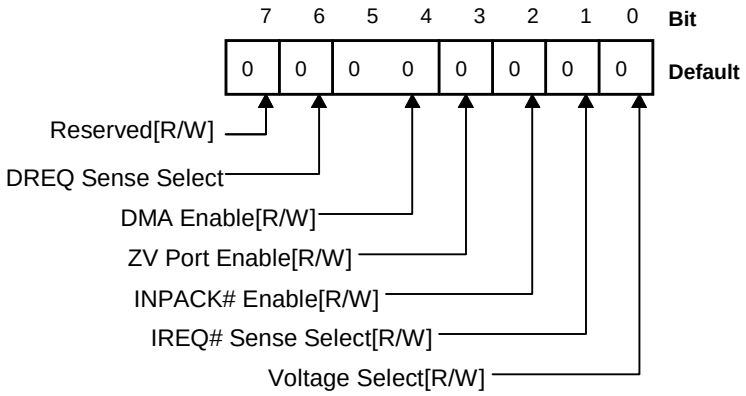


Bit	Field Name	Description
7-3	ATAaddressA25..A21	This field contains the card address 25-21 in PCMCIA-ATA mode. This field has no effect excepting this meaning.
2	Reserved(R/W)	This read/write bit is reserved.
1	LEDenable	When this bit is set to1, IRQ12 becomes open drain output suitable for driving an LED (driven whenever the card-SPKR output is turned on, and corresponding SPKR# is LED input bit is set). This bit works independent of Bit 0 (ATA mode).
0	ATAmode	When this bit is set to 1, PCMCIA-ATA mode is selected.

7.8.2 Misc Control 1 register

This register controls the miscellaneous signals like INPCK# and IREQ# for the PC Card-16.

Register Name: Miscellaneous Control 1
Address Offset: 82Fh (8 bit)

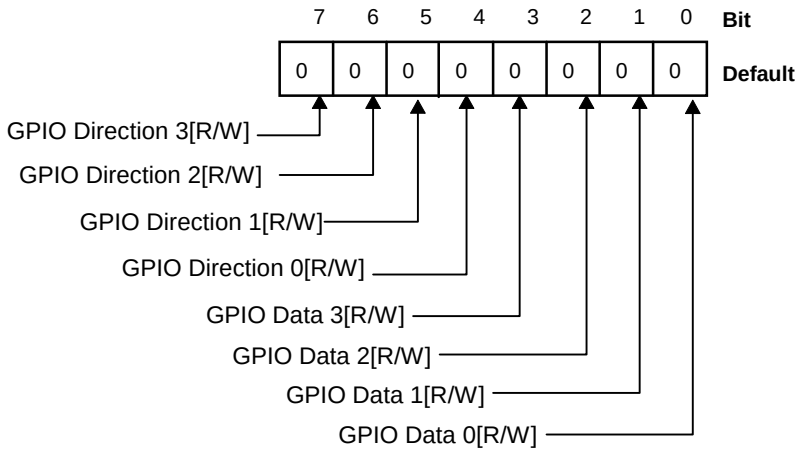


Bit	Field Name	Description
7	Reserved(R/W)	This read/write bit is reserved for future use.
6	DREQ Sense Select	When this bit is set to 1, the DREQ# signal is “high” active. When this bit is set to 0, the DREQ# signal is “low” active. The default after reset is zero.
5-4	DMA Enable	This field determines which signal asserted as the DREQ signal, at the same time DMA mode is enabled. The default is this field returns zero and DMA mode is disabled. 00 DMA disabled 01 INPACK# is assigned as DREQ. 10 WP/IOIS16# is assigned as DREQ. 11 BVD2/SPKR# is assigned as DREQ.
3	ZV Port Enable	When this bit is set to 1, the PC Card-16 interface is Zoomed Video Port mode. Therefore, the card address lines CADR[25:4] are put in tri-state, and then replaced by Zoomed Video Port signals, with BVD2/SPKR# and INPACK#, which carry video/audio data from the PC Card-16 to the ZV port. The default is zero.
2	INPACK# Enable	When this bit is set to 1, the INPACK# signal is enabled on the PC Card-16 interface. The 5C475 returns ones on I/O read unless INPACK# is asserted, and ends normally. When this bit is set to 0, the INPACK# signal is disabled.
1	IREQ# Sense Select	When this bit is set to 1, the IREQ# signal is “high” active. When this bit is set to 0, the IREQ# signal is “low” active.
0	Voltage Select	This bit is used with Bit4-0 in the Power Control register in order to control the Socket voltage. The setting is described in Power Control Register section.

7.8.3 General Purpose I/O register

This register contains the general purpose I/O signals. IRQ3,4,5 and 7 asserted to GPIO(General Purpose I/O) pins can be determined by user without effect on the controller transaction. The default is input mode. The state of this register which is input can be read by Bit 3-0. The state of each bits in this register which is output are output through GPIO 3-0 pins.

Register Name: General Purpose I/O
Address Offset: 83Ah (8 bit)



Bit	Field Name	Description
7	GPIO Direction 3	GPIO Data 3 I/O change signal. When this bit is set to 0, GPIO Data 3 is input. When this bit is set to 1, CPIO Data 3 is output. The default is zero.
6	GPIO Direction 2	GPIO Data 3 I/O change signal. When this bit is set to 0, GPIO Data 2 is input. When this bit is set to 1, CPIO Data 2 is output. The default is zero.
5	GPIO Direction 1	GPIO Data 3 I/O change signal. When this bit is set to 0, GPIO Data 1 is input. When this bit is set to 1, CPIO Data 1 is output. The default is zero.
4	GPIO Direction 0	GPIO Data 3 I/O change signal. When this bit is set to 0, GPIO Data 0 is input. When this bit is set to 1, CPIO Data 0 is output. The default is zero.
3	GPIO Data 3	General Purpose I/O bit 3. The default is input.
2	GPIO Data 2	General Purpose I/O bit 2. The default is input.
1	GPIO Data 1	General Purpose I/O bit 1. The default is input.
0	GPIO Data 0	General Purpose I/O bit 0. The default is input.

7.9 PCIway DMA Operation Registers

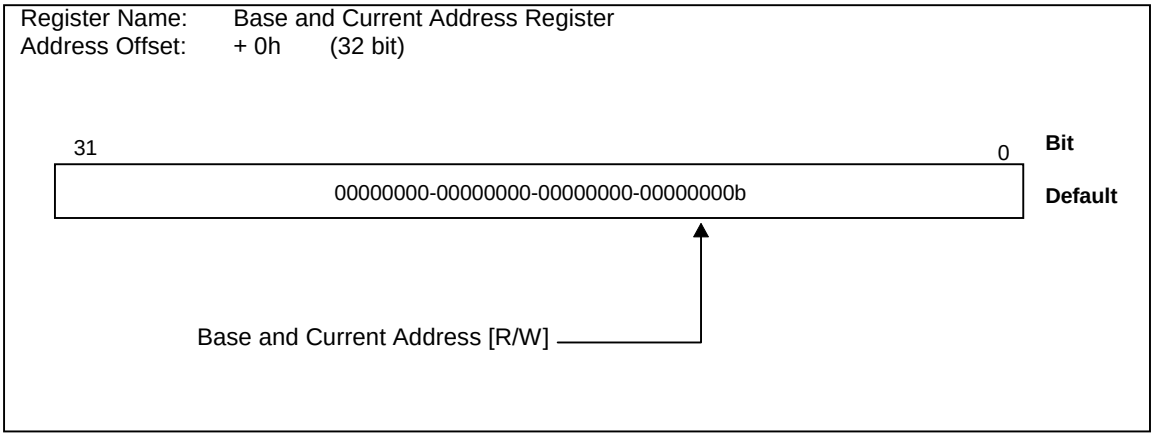
The 5C475 supports PCIway DMA operation in order to maintain the compatibility with the existing 16-bit card using ISA DMA operation. The DMA slave channel has a block of 8, 16 bit registers, defined below. This block is locatable anywhere in the legacy 64k I/O space, by programming the DMA Slave Configuration Register. All registers are I/O registers offset from the base address loaded in the DMA Slave Configuration register.

Slave Address	R/W	Register Name
base + 0h	W	Base Address 0-7
base + 0h	R	Current Address 0-7
base + 1h	W	Base Address 8-15
base + 1h	R	Current Address 8-15
base + 2h	W	Base Address 16-23
base + 2h	R	Current Address 16-23
base + 3h	W	Base Address 24-31
base + 3h	R	Current Address 24-31
base + 4h	W	Base Word Count 0-7
base + 4h	R	Current Word Count 0-7
base + 5h	W	Base Word Count 8-15
base + 5h	R	Current Word Count 8-15
base + 6h	W	Base Word Count 16-23
base + 6h	R	Current Word Count 16-23
base + 7h	N/A	Reserved
base + 8h	W	Command
base + 8h	R	Status
base + 9h	W	Request
base + Ah	N/A	Reserved
base + Bh	W	Mode
base + Ch	W	Reserved
base + Dh	W	Master Clear
base + Eh	N/A	Reserved
base + Fh	R/W	Multi-Channel Mask

Programming Model for Single DMA Slave Channel

7.9.1 Base and Current Address register

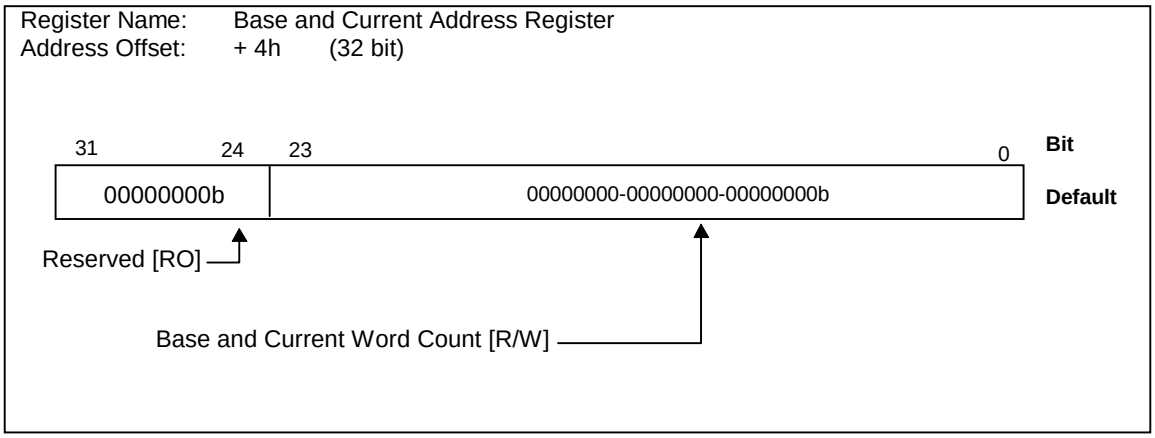
This register is used to form part of the address for DMA transfers. The function of this register is the same as for legacy DMA. This register corresponds to the Base Address register of the 8237 for write operations. This register contains the Current address for read operations.



Bit	Field Name	Description
31-24	High Address	This bit field corresponds to the Base Address register of 8237 for write operations. This register contains the Current address for read operations. This bit field corresponds to the base and current address bit[31:24]. This field is reset to 00h during DMA transfers from the 5C475 to memory unless Non Legacy Extended Addressing bit in DMA Slave Configuration register is set to one. The default is 00h.
23-16	Mid High Address	This bit field corresponds to the Base Address register of 8237 for write operations. This register contains the Current address for read operations. When 8-bit transfer mode is selected in DMA Slave Configuration register, this bit field contains the starting address bits[23:16]. When 16-bit transfer mode is selected in the DMA Slave Configuration register, this bit field contains the starting address bits[23:17] and Bit 16 of this field is not used for anything. The default is 00h.
15-8	Mid Low Address	This bit field corresponds to the Base Address register of 8237 for write operations. This register contains the Current address for read operations. When 8-bit transfer mode is selected in DMA Slave Configuration register, this bit field contains the starting address bits[15:8]. When 16-bit transfer mode is selected in the DMA Slave Configuration register, this bit field contains the starting address bits[16:9]. The default is 00h.
7-0	Low Address	This bit field corresponds to the Base Address register of 8237 for write operations. This register contains the Current address for read operations. When 8-bit transfer mode is selected in DMA Slave Configuration register, this bit field contains the starting address bits[7:0]. When 16-bit transfer mode is selected in the DMA Slave Configuration register, this bit field contains the starting address bits[8:1]. The default is 00h.

7.9.2 Base and Current Word Count register

This register corresponds to the Base Count of the 8237 for write operations. This register corresponds to the Current Word Count register for read operations. DMA transfers are counted by transaction, not by byte, word, or double word. The count registers count down from the programmed value to zero and then one more. Therefore this written register is the total count of transactions plus one, and reads out the number of reaming transactions when read.

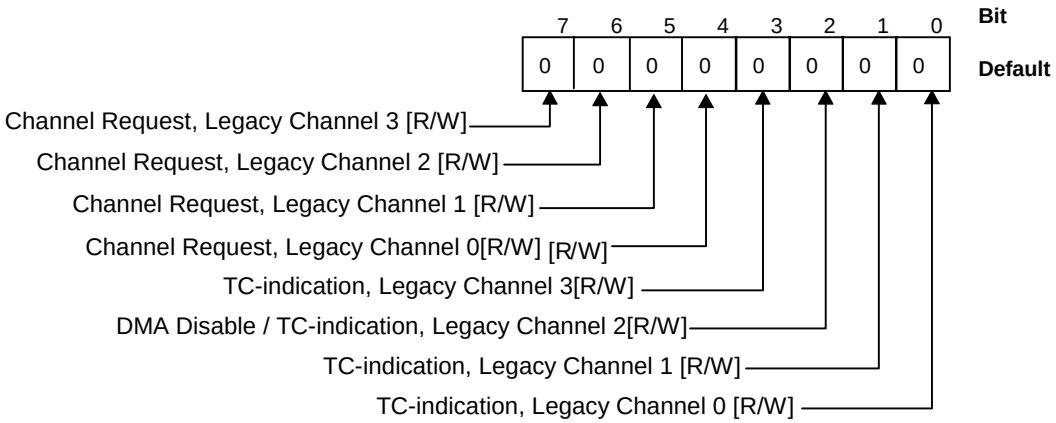


Bit	Field Name	Description
31-24	Reserved	This field is reserved and returns zero when read.
23-16	High Count	This field can be used to increase the total number of transfers above original 64K transfers of the 8237 when Non Legacy Extended Addressing bit in the DMA Slave Configuration register is set to one. The default is 00h.
15-8	Mid Count	This field corresponds to the Base Count register of the 8237 for write operations. This field corresponds to the Current Word Count register for read operations. The default is 00h.
7-0	Low Count	This field corresponds to the Base Count register of the 8237 for write operations. This field corresponds to the Current Word Count register for read operations. The default is 00h.

7.9.3 Command and Status register

The function of the Command register is the same as for Legacy DMA, which also means that Memory to Memory functionality is not supported because it is not supported in a Legacy PC. Writing to this register has no meaning except for Bit 2. The 5C475 returns the same TC indication on bit[3:0] and the same channel request on bit[7:4] as the DMA slave during status read. It is the DMA Master's responsibility to properly assemble the contents of this register.

Register Name: Command and Status Register
Address Offset: + 8h (8 bit)

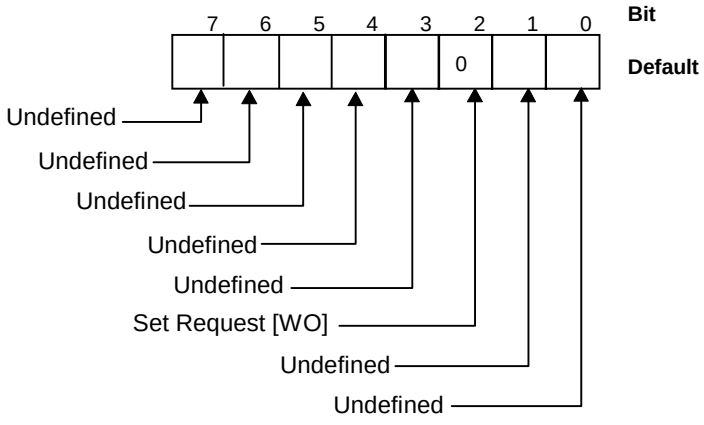


Bit	Field Name	Description
7	Channel Request 3	Writing to this bit has no meaning. Returns PC Card DMA request line inverted When read. The Default is zero.
6	Channel Request 2	Writing to this bit has no meaning. Returns PC Card DMA request line inverted When read. The Default is zero.
5	Channel Request 1	Writing to this bit has no meaning. Returns PC Card DMA request line inverted When read. The Default is zero.
4	Channel Request 0	Writing to this bit has no meaning. Returns PC Card DMA request line inverted When read. The Default is zero.
3	TC indication 3	Writing to this bit has no meaning. Returns TC when read. The default is zero.
2	DMA disable/ TC indication 2	When this bit is set to one, DMA transfer is disabled. Returns TC when read. The default is zero.
1	TC indication 1	Writing to this bit has no meaning. Returns TC when read. The default is zero.
0	TC indication 0	Writing to this bit has no meaning. Returns TC when read. The default is zero.

7.9.4 Request register

The function of the Request register is the same as that of the 8237. Read from this register are undefined and only the Set Request bit has the meaning for this implementation.

Register Name: Request Register
Address Offset: + 9h (8 bit)

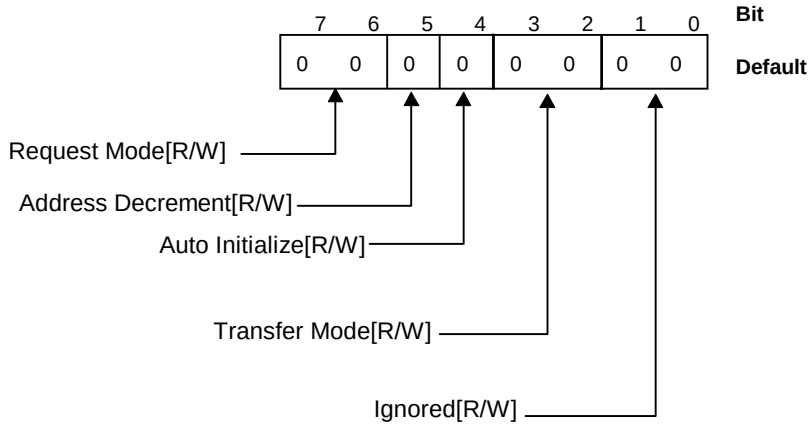


Bit	Field Name	Description
7-3	Undefined	Returns zero when read.
2	Set Request	When the transfer mode bits are set to the block transfer mode, this bit initiates transfers with no hardware request present on the PC Card interface.
1-0	Undefined	Returns zero when read.

7.9.5 Mode Register

This register emulates the mode register of the 8237. This register, unlike the 8237 mode register, is readable.

Register Name: Mode Register
Address Offset: + Bh (8 bit)

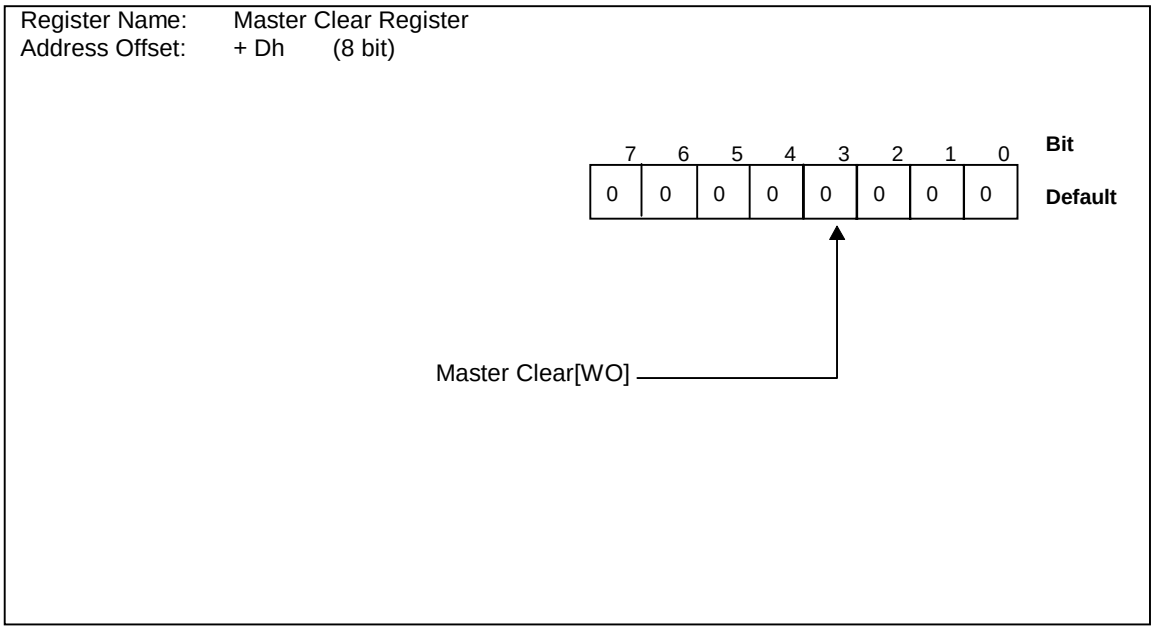


Bit	Field Name	Description
7-6	Request Mode	This bit field determines the request mode to be used. The default is zero. 00 Demand Mode 01 Single Transfer Mode 10 Block Mode Select 11 not implemented
5	Address Decrement	When this bit is set to one, the address is generated by proceeding downward from the base address until the count is exhausted. When this bit is reset, the address is generated by increment until the end of transfer. The default is zero.
4	Auto Initialize	When this bit is set to one, the DMA controller is put in autoinitialize mode. In this mode the Current address and count registers are reloaded form the Base registers. This sets the DAM controller up to do a new transfer at the end of the current transfer. The default is zero.
3-2	Transfer Mode	This bit field determines the transfer mode to be used. The default is zero. 00 Verify Mode (does DMA Write at PC card interface) 01 DMA Write 10 DMA Read 11 Reserved
1-0	Ignored	This field is Scratch bits. The default is zero.

7.9.6 Master Clear register

This register emulates the Master Clear register of the8237. The 5C475 has no temporary register to read back, unlike the 8237, so read back is not supported. When this register is written the DMA section of the 5C475 assumes the same state as caused by PCI_RESET#. The data is “don’t care”. The DMA Slave configuration register is not affected by writing to this register.

Register Name: Master Clear Register
Address Offset: + Dh (8 bit)

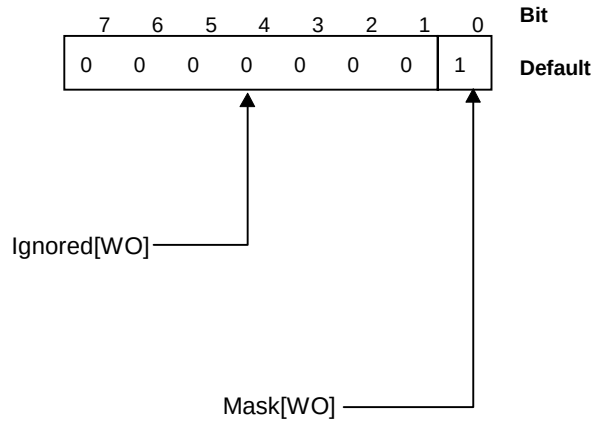


Bit	Field Name	Description
7-0	Master Clear	When this register is written the DMA section of the 5C475 assumes the same state as caused by PCI_RESET#. The DMA Slave Configuration register is not affected by writing to this register. The default is zero.

7.9.7 Mask register

This register emulates the Mask registers of the 8237. The 5C475, unlike the 8237, supports only one channel represented here. Read back is supported. When this bit is one, the DREQ signal from the PC Card is ignored. And when this bit is zero, DMA requests are enabled. This bit is automatically set unless Autoinitilize bit is set when a transfer completes.

Register Name: Mask Register
Address Offset: + Fh (8 bit)



Bit	Field Name	Description
7-1	Ignored	Writing this bit has no meaning. The default is zero.
0	Mask	When this bit set to one, the DREQ signal is ignored. When this bit is set to zero, DMA requests are enabled. This bit is automatically set unless Autoinitilize bit is set when a transfer completes.

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum rating

Symbol	Parameter	Min	Unit	Condition	note
Vcc 1	Supply Voltage Range 1	-0.3 ~ 6.6	V	GND=0V	1
Vcc 2	Supply Voltage Range 2	-0.3 ~ 5.0	V	GND=0V	2
Vte	Voltage on Any Pin	-0.3 ~ Vcc+0.3	V	GND=0V	
Topr	Ambient Temperature under bias	-40 ~ 85	˚C		
Tstg	Storage Temperature Range	-55 ~ 125	˚C		

note 1 : Applied for Vcc_xxx except for Vcc_core .
note 2 : Applied for Vcc_core only.

Note: Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

8.2 DC Characteristics

8.2.1 Recommended Operating Conditions for Power Supply

Power Pin	Parameter	Min	Typ	Max	Unit	Note
VCC_PCI	Supply Voltage for PCI interface (5.0V Operation)	4.75	5.0	5.25	V	
VCC_PCI	Supply Voltage for PCI interface (3.3V Operation)	3.0	3.3	3.6	V	
VCC_CORE	Supply Voltage for Core Logic	3.0	3.3	3.6	V	
VCC_5V	Supply Voltage for 5V Control Signals	3.0	5.0	5.25	V	
VCC_SLOT A	Supply Voltage for Card Socket A (5.0V Operation)	4.75	5.0	5.25	V	
VCC_SLOT A	Supply Voltage for Card Socket A (3.3V Operation)	3.0	3.3	3.6	V	

8.2.2 PCI Interface

For 5V signaling

(VCC_CORE=3.0~3.6V, VCC_PCI=4.75~5.25V, Ta=0~70˚C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VIH	Input High Voltage	2.0	Vcc_PCI +0.5	V		1
VIL	Input Low Voltage	-0.5	0.8	V		1
VOH	Output High Voltage	2.4		V	Iout=-2mA	1
VOL	Output Low Voltage		0.55	V	Iout=6mA	1
IIH	Input High Leakage Current		70	μA	Vin=2.7V	1
IIL	Input Low Leakage Current		-70	μA	Vin=0.5V	1
Cin	Input Pin Capacitance		10	pF		1
Cclk	PCICLK Pin Capacitance		12	pF		1

For 3.3V signaling

(VCC_CORE=3.0~3.6V, VCC_PCI=3.0~3.6V, Ta=0~70˚C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VIH	Input High Voltage	0.5Vcc_PCI	Vcc_PCI+0.5	V		1
VIL	Input Low Voltage	-0.5	0.3Vcc_PCI	V		1
VOH	Output High Voltage	0.9Vcc_PCI		V	Iout=-500μA	1
VOL	Output Low Voltage		0.1Vcc_PCI	V	Iout=1500μA	1
IILk	Input Leakage Current		±10	μA	Vin=0~Vcc_PCI	1
Cin	Input Pin Capacitance		10	pF		1
Cclk	PCICLK Pin Capacitance		12	pF		1

Note 1: Applied for PCICLK, CLKRUN#, PCIRST#, AD[31:0], C/BE#[3:0], PAR, FRAME#, IRDY#, TRDY#,STOP#, DEVSEL#, IDSEL, PERR#, SERR#, REQ#, GNT#, INTA# pins

8.2.3 16-bit PC Card Interface

For 5V signaling

(VCC_CORE=3.0~3.6V, VCC_SLOTA =4.75~5.25V, Ta=0~70˚C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH	Input High Voltage	2.4		Vcc_SLOT +0.3	V		2
VIL	Input Low Voltage	-0.3		0.8	V		2
VOH1	Output High Voltage	2.4			V	Iout=-8mA	2
VOH2	Output High Voltage	2.4			V	Iout=-4mA	2,3
VOL1	Output Low Voltage			0.4	V	Iout=8mA	2
VOL2	Output Low Voltage			0.4	V	Iout=4mA	2,3
IILk	Input Leakage Current			±10	μA	Vin=0~Vcc_SLOTA	2
IIL1	Input Leakage Current (Pull-up)		-120		μA	Vin=0	2,4
Cin	Input Pin Capacitance			10	pF		2

For 3.3V signaling

(VCC_CORE=3.0~3.6V, VCC_SLOTA =3.0~3.6V, Ta=0~70˚C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH	Input High Voltage	2.0		Vcc_SLOT +0.3	V		2
VIL	Input Low Voltage	-0.3		0.6	V		2
VOH1	Output High Voltage	2.4			V	Iout=-4mA	2
VOH2	Output High Voltage	2.4			V	Iout=-2mA	2,3
VOL1	Output Low Voltage			0.4	V	Iout=4mA	2
VOL2	Output Low Voltage			0.4	V	Iout=2mA	2,3
IILk	Input Leakage Current			±10	μA	Vin=0~Vcc_SLOTA	2
IIL1	Input Leakage Current (Pull-up)		-50		μA	Vin=0	2,4
Cin	Input Pin Capacitance			10	pF		2

Note 2: Applied for CADR[25:0], CDATA[15:0], CE[2:1]#, IOR#, IOW#, OE#, WE#, REG#, RDY/IREQ#, WAIT#, WP/IOIS16#, RESET, BVD1/STSCHG#/RI#, BVD2/SPKR#, INPACK# pins, if Card interface is configured as a 16-bit Card Socket.

Note 3: Applied for RESET pins

Note 4: Applied for RDY/IREQ#, WAIT#, BVD1/STSCHG#/RI#, BVD2/SPKR#, INPACK# pins

8.2.4 CardBus PC Card Interface

(VCC_CORE=3.0~3.6V, VCC_SLOTA =3.0~3.6V, Ta=0~70˚C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH	Input High Voltage	0.475x Vcc_SLOTA		Vcc_SLOT +0.5	V		5
VIL	Input Low Voltage	-0.5		0.325x Vcc_SLOT	V		5
VOH	Output High Voltage	0.9Vcc_SLOTA			V	Iout=-150μA	5
VOL	Output Low Voltage			0.1Vcc_SLOT	V	Iout=700μA	5
IILk	Input Leakage Current			±10	μA	Vin=0~Vcc_SLOTA	5
IIL1	Input Leakage Current (Pull-up)		-230		μA	Vin=0	5,6
IIL2	Input Leakage Current (Pull-down)		10		μA	Vin=Vcc_SLOTA	2,7
Cin	Input Pin Capacitance			10	pF		5

Note 5: Applied for CCLK, CCLKRUN#, CRST#, CAD[31:0], CC/BE#[3:0], CPAR, CFRAME#, CIRDY#,CTRDY#,CSTOP#, CDEVSEL#, CBLOCK#, CPERR#, CSERR#, CREQ#, CGNT#, CINT#, CAUDIO, CSTSCHG pins, if Card interface is configured as a CardBus Card Socket.

Note 6 : Applied for CCLKRUN#, CIRDY#,CTRDY#,CSTOP#, CDEVSEL#, CPERR#, CSERR#, CREQ#, CINT#, CAUDIO pins

Note 7 : Applied for CSTSCHG pins

8.2.5PC Card Interface Card detect Pins and System Interface Pins

PC Card Interface Card Detect Pins and System Interface Pins

(VCC_CORE=3.0~3.6V, VCC_5V=4.75~5.25V, Ta=0~70˚C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH	Input High Voltage	2.4		Vcc_5V+0.3	V		9,11
VIL	Input Low Voltage	-0.3		0.8	V		9,11
VOH1	Output High Voltage	2.4			V	Iout=-4mA	10
VOH2	Output High Voltage	2.4			V	Iout=-1mA	11
VOL1	Output Low Voltage			0.4	V	Iout=4mA	10
VOL2	Output Low Voltage			0.4	V	Iout=1mA	11
IILk	Input Leakage Current			±10	μA	Vin=0~Vcc_5V	11
IIL1	Input Leakage Current (Pull-up)		-140		μA	Vin=0	9
IOZ	Hi-Z Output Leakage Current			±10	μA	Vout=0~Vcc_5V	10

Note 9: Applied for CD1#(CCD1#), CD2#(CCD2#) pins

Note 10: Applied for RI_OUT#, SPKROUT#,VCC5EN#, VCC3EN#, VPPEN0, VPPEN1 pins

Note 11: Applied for VS1#(CVS1#), VS2#(CVS2#), pins

8.2.6 IRQ3-15 pin

For PCI 5V signaling

(VCC_CORE=3.0~3.6V, VCC_PCI=4.75~5.25V, Ta=0~70˚C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VOH	Output High Voltage	2.4		V	Iout=-8mA	12
VOL	Output Low Voltage		0.4	V	Iout=8mA	12
IOZ	Hi-Z Output Leakage Current		±10	μA	Vout=0~Vcc_PCI	12

For PCI 3.3V signaling

(VCC_CORE=3.0~3.6V, VCC_PCI=3.0~3.6V, Ta=0~70˚C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VOH	Output High Voltage	2.4		V	Iout=-4mA	12
VOL	Output Low Voltage		0.4	V	Iout=4mA	12
IOZ	Hi-Z Output Leakage Current		±10	μA	Vout=0~Vcc_PCI	12

Note 12: Applied for IRQ3-15 pins

8.2.7 Power Consumption

Power Supply Current

Power Pin	Parameter	Min	Typ	Max	Unit	Condition
Iccstd	Power Supply Current, Standby			50	μA	fclk(PCICLK)=0, Vin=0or Vcc
Iccsusp	Power Supply Current, Hardware Suspend Mode			30	μA	Mode = H/W Bridge Suspend VCC_SLOT=5.0V VCC_5V=5.0V VCC_PCI=0V VCC_CORE=3.3V Vin=0 or Vcc
Icc	Power Supply Current, Operating			40	mA	fclk(PCICLK)=33Mhz VCC_SLOT=5.0/3.3V VCC_5V=5.0V VCC_PCI=5.0V VCC_CORE=3.3V Vin=0 or Vcc

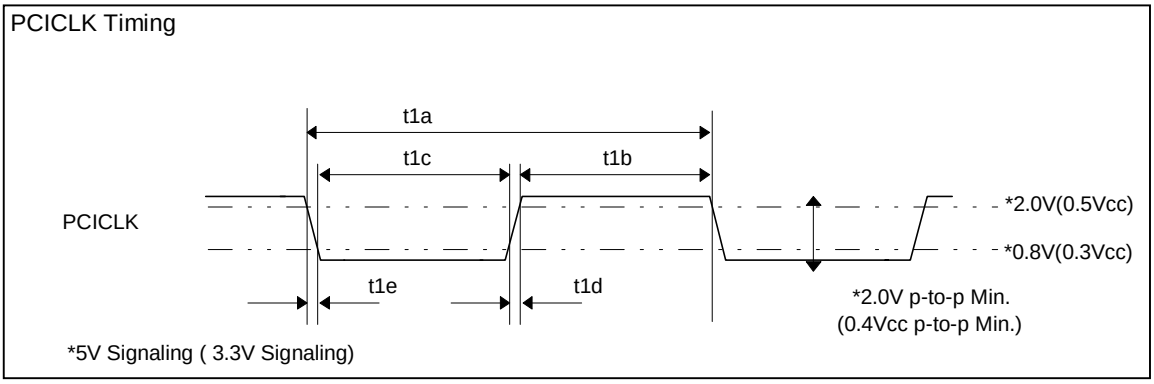
8.3 AC Characteristics

8.3.1 PCI Interface Signals

PCI Clock

(VCC_CORE=3.0~3.6V, VCC_PCI=3.0~3.6V or 4.75~5.25V, Ta=0~70˚C)

Symbol	Parameter	Min	Max	Unit	Notes
	PCICLK				
t1a	Cycle Time, PCICLK	30		ns	
t1b	Pulse Width Duration, PCICLK High	11		ns	
t1c	Pulse Width Duration, PCICLK Low	11		ns	
t1d	Slew Rate, PCICLK Rising Edge	1	4	V/ns	
t1e	Slew Rate, PCICLK Falling Edge	1	4	V/ns	

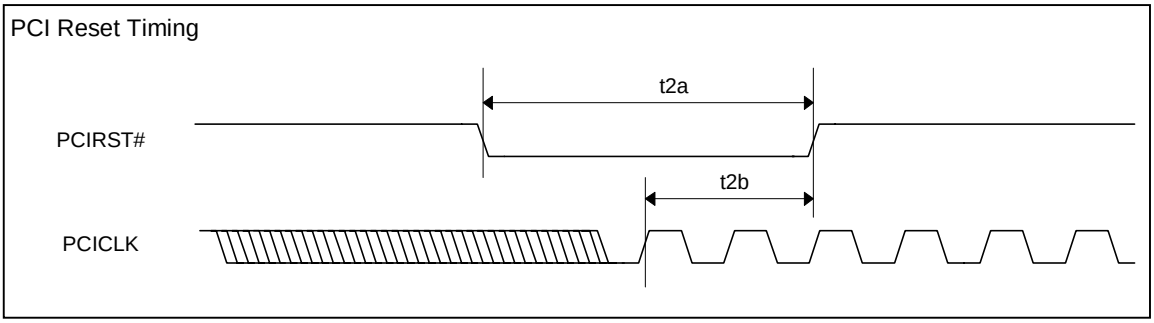


PCICLK Timing

PCI Reset

(VCC_CORE=3.0~3.6V, VCC_PCI=3.0~3.6V or 4.75~5.25V, Ta=0~70˚C)

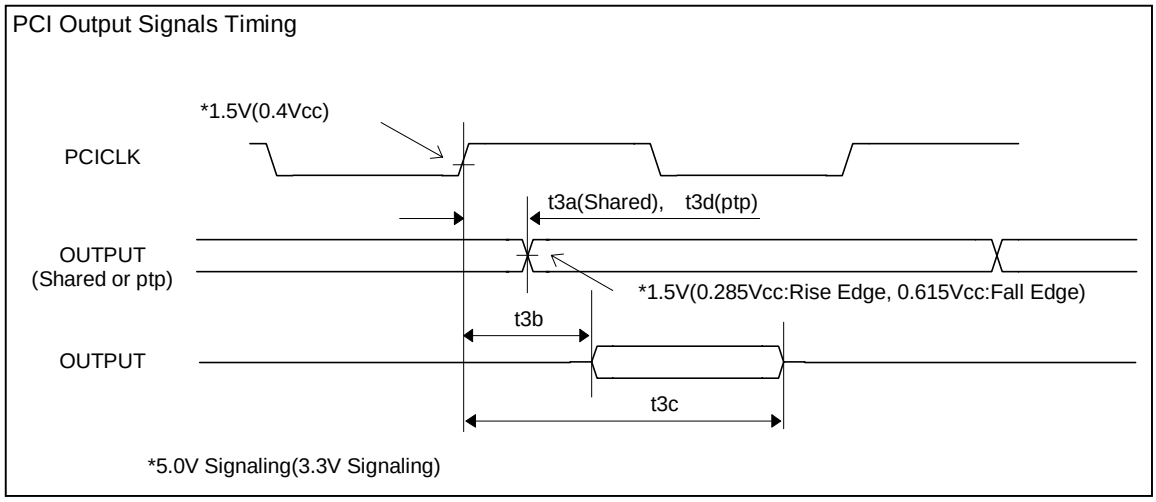
Symbol	Parameter	Min	Max	Unit	Notes
	PCIRST#				
t2a	Pulse Duration, PCIRST#	1		ms	
t2b	Setup Time,PCICLK active at PCIRST# Negation	100		µs	



PCI Reset Timing

PCI Interface Output Signals
(VCC_CORE=3.0~3.6V, VCC_PCI=3.0~3.6V or 4.75~5.25V, Ta=0~70˚C)

Symbol	Parameter	Min	Max	Unit	Notes
	AD[31:0], C/BE#[3:0], PAR, FRAME#,DEVSEL#, IRDY#, TRDY#,STOP#, PERR#, SERR#, CLKRUN#				
t3a	Shared Signal Valid delay time from PCICLK	2	11	ns	Min: CL=0 pF Max: CL=50 pF (10 pF 3.3v)
t3b	Enable Time, Hi-Z to active delay from PCICLK	2		ns	
t3c	Disable Time, Active to Hi-Z delay from PCICLK		28	ns	
	REQ#				
t3d	Point to Point Signal Valid delay time from PCICLK	2	12	ns	Min: CL=0 pF Max: CL=50 pF (10 pF 3.3v)

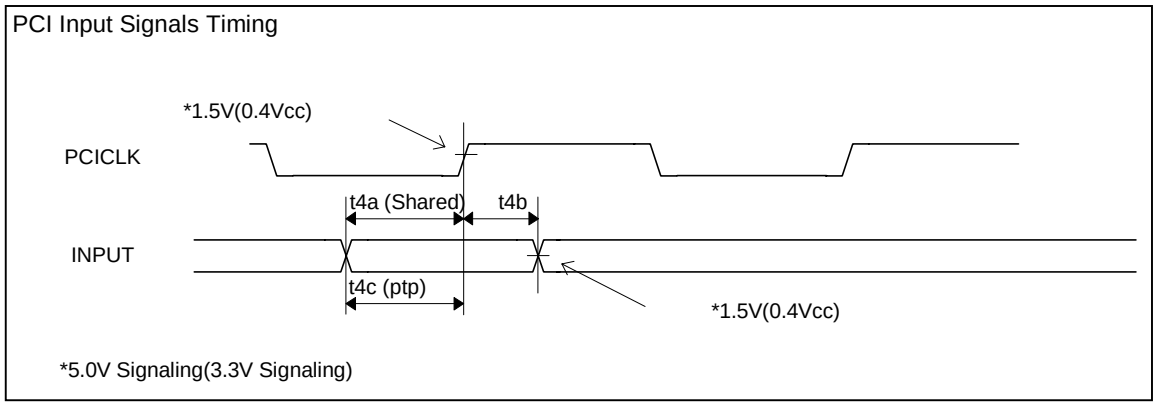


PCI Output Signals Timing

PCI Interface Input Signals

(VCC_CORE=3.0~3.6V, VCC_PCI=3.0~3.6V or 4.75~5.25V, Ta=0~70˚C)

Symbol	Parameter	Min	Max	Unit	Notes
	CAD[31:0], C/BE#[3:0], PAR, FRAME#,DEVSEL#, IRDY#, TRDY#,STOP#, IDSEL, PERR#, SERR#, CLKRUN#				
t4a	Setup Time, Shared Signal Valid before PCICLK	7		ns	
t4b	Hold Time,Shared Signal Hold Time after PCICLK High	0		ns	
	GNT#				
t4c	Setup Time, Point to Point Signal Valid before PCICLK	10		ns	



PCI Input Signals Timing

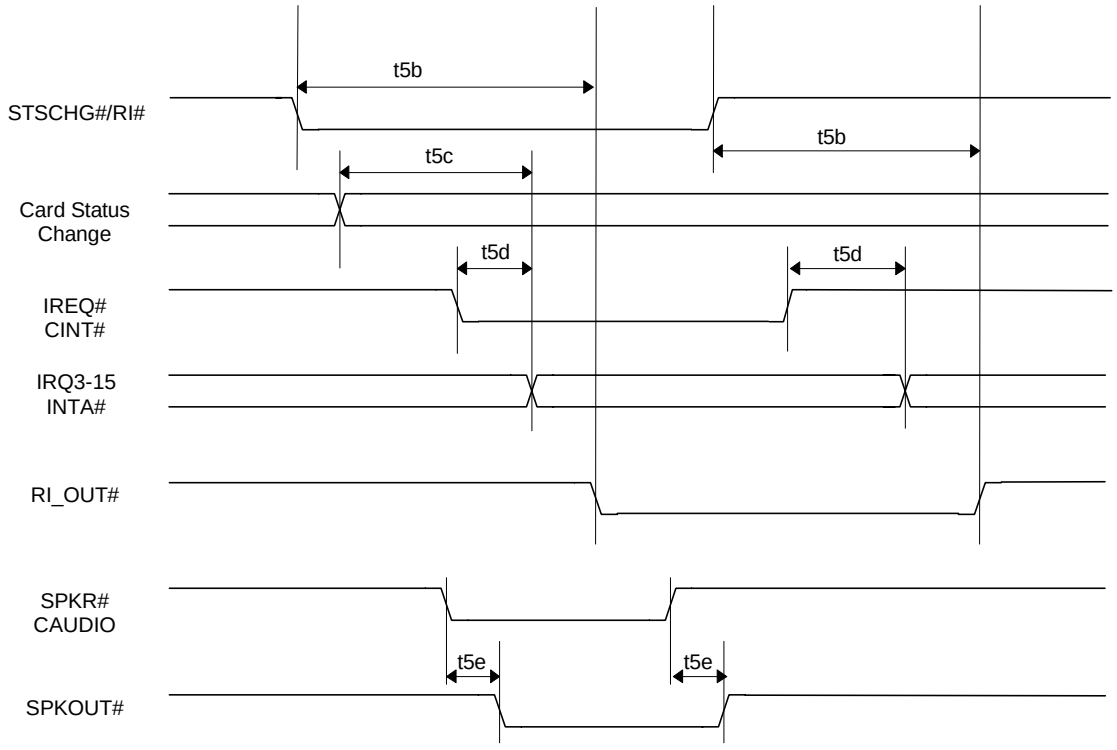
8.3.2 System Interface Signals

System Interface Signals AC Characteristics
(VCC_CORE=3.0~3.6V, VCC_PCI=3.0~3.6V or 4.75~5.25V, VCC_SLOTA=3.0~3.6V or 4.75~5.25V, VCC_5V= 4.75~5.25V,Ta=0~70˚C)

Symbol	Parameter	Min	Max	Unit	Notes
	RI_OUT#, IRQ3-15, INTA#				
t5b	RI# to RI_OUT# Delay		50	ns	
t5c	Card Status Change to IRQ3-15/INTA# Delay		2Tcyc+0	ns	1
t5d	Card IREQ#/CINT# to IRQ3-15/INTA# Delay		50	ns	
	SPKOUT#				
t5e	SPKR#/CAUDIO to SPKOUT# Delay		50	ns	

Note1: Tcyc is PCICLK cycle time.(Typically 30ns)

System Signals Timing



System Signals Timing

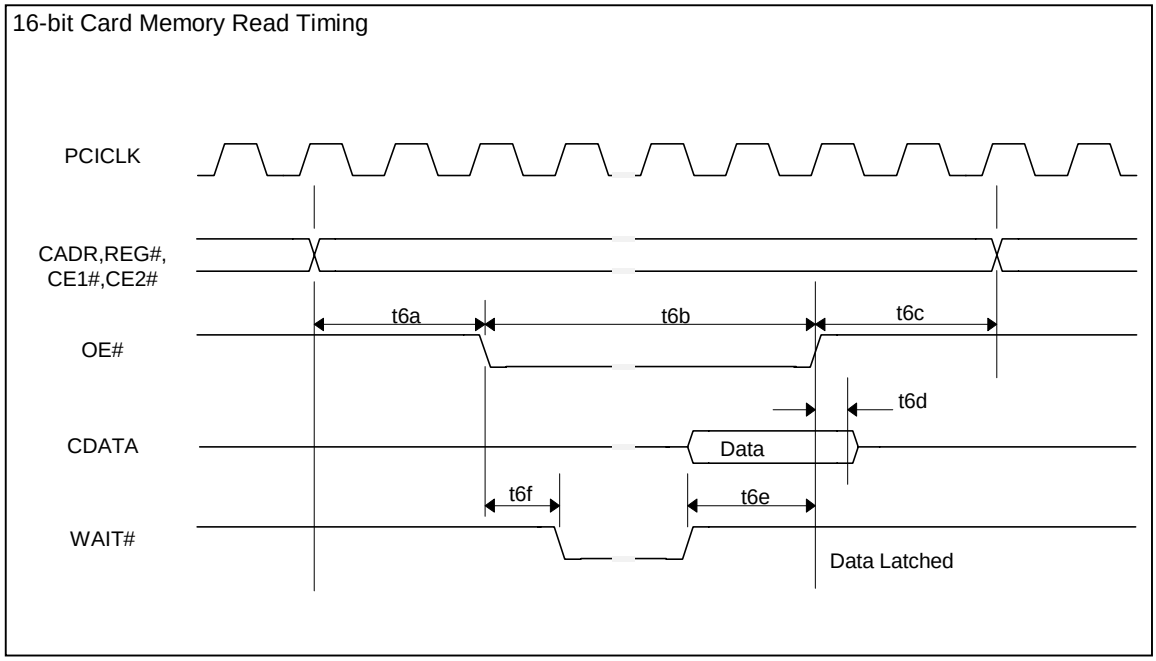
8.3.3 16-bit PC Card Interface Signals

Memory Read

(VCC_CORE=3.0~3.6V, VCC_SLOTA=3.0~3.6V or 4.75~5.25V, Ta=0~70˚C)

Symbol	Parameter	Min	Max	Unit	Notes
	CADR[25:0], REG#, CE[2:1]#				
t6a	Setup Time, CADR[25:0], REG# and CE[2:1]# before OE# Low	Tsu-20		ns	1,2 Tsu=1~7Tcyc Programmable
t6c	Hold Time, CADR[25:0], REG# and CE[2:1]# after OE# High	Thl-10		ns	1,2 Thl=1~7Tcyc Programmable
	OE#				
t6b	Pulse Duration, OE# Low	Tpw-20		ns	1,2 Tpw=3~31Tcyc Programmable
	CDATA[15:0]				
t6d	Hold Time, CDATA[15:0] after OE# High	0		ns	
	WAIT#				
t6e	Hold Time, OE# Low after WAIT# High	1Tcyc+0		ns	1
t6f	Valid Delay, OE# Low to WAIT# Low		50	ns	

Note1: Tcyc is PCICLK cycle time.(Typically 30ns)
Note2: Tsu, Tpw, Thl can be programmed by setting 16-bit Memory Timing 0 register.



16-bit Card Memory Read Timing

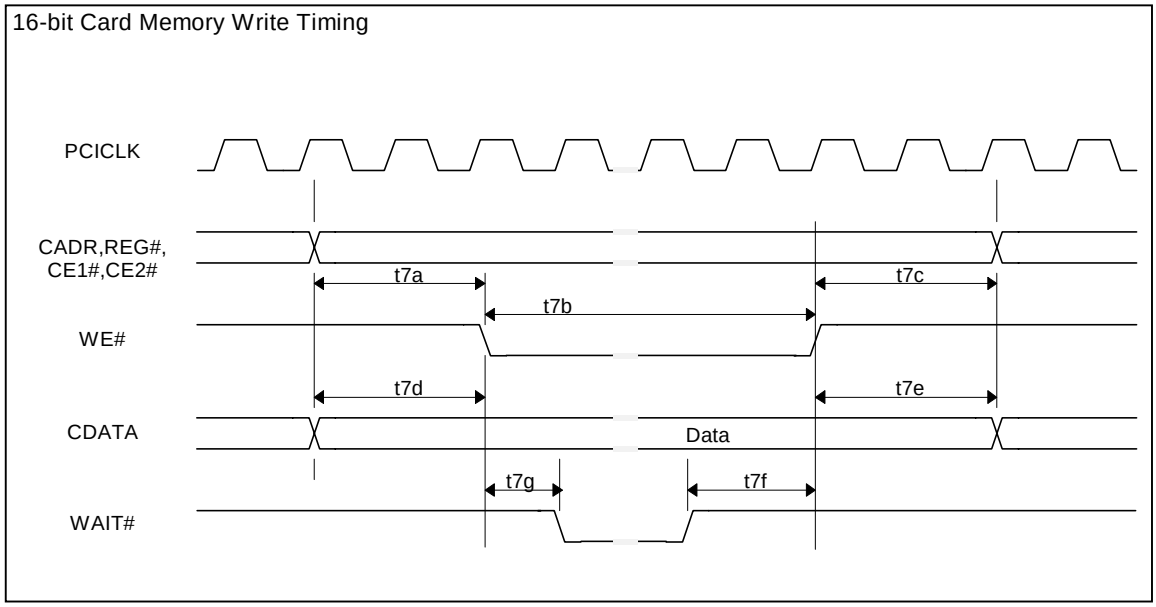
Memory Write

(VCC_CORE=3.0~3.6V, VCC_SLOTA=3.0~3.6V or 4.75~5.25V, Ta=0~70˚C)

Symbol	Parameter	Min	Max	Unit	Notes
	CADR[25:0], REG#, CE[2:1]#				
t7a	Setup Time, CADR[25:0], REG# and CE[2:1]# before WE# Low	Tsu-20		ns	1,2 Tsu=1~7Tcyc Programmable
t7c	Hold Time, CADR[25:0], REG# and CE[2:1]# after WE# High	Thl-10		ns	1,2 Thl=1~7Tcyc Programmable
	WE#				
t7b	Pulse Duration, WE# Low	Tpw-20		ns	1,2 Tpw=3~31Tcyc Programmable
	CDATA[15:0]				
t7d	Setup Time, CDATA[15:0] before WE# Low	Tsu-20		ns	1,2 Tsu=1~7Tcyc Programmable
t7e	Hold Time, CDATA[15:0] after WE# High	Thl-10		ns	1,2 Thl=1~7Tcyc Programmable
	WAIT#				
t7f	Hold Time, WE# Low after WAIT# High	Tcyc+0		ns	1
t7g	Valid Delay, WE# Low to WAIT# Low		50	ns	

Note1: Tcyc is PCICLK cycle time.(Typically 30ns)

Note2: Tsu, Tpw, Thl can be programmed by setting 16-bit Memory Timing 0 register.



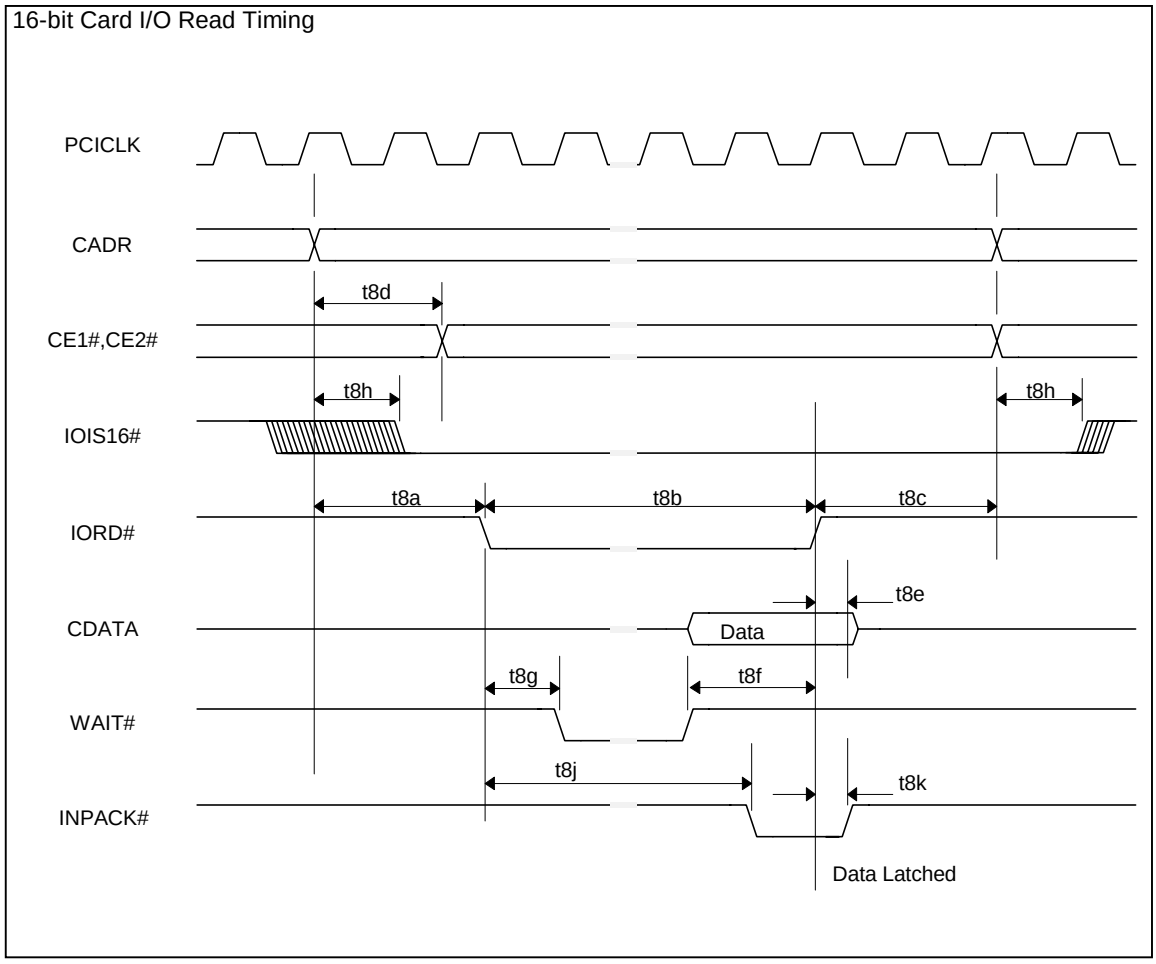
16-bit Card Memory Write Timing

I/O Read

(VCC_CORE=3.0~3.6V, VCC_SLOTA=3.0~3.6V or 4.75~5.25V, Ta=0~70˚C)

Symbol	Parameter	Min	Max	Unit	Notes
	CADR[25:0], REG#				
t8a	Setup Time, CADR[25:0] and REG# before IORD# Low	Tsu-20		ns	1,3 Tsu=2~7Tcyc Programmable
t8c	Hold Time, CADR[25:0] and REG# after IORD # High	Thl-10		ns	1,3 Thl=1~7Tcyc Programmable
	IORD#				
t8b	Pulse Duration, IORD # Low	Tpw-20		ns	1,3 Tpw=3~31Tcyc Programmable
	CE[2:1]#				
t8d	Valid Delay, CADR[15:0] and REG# to CE[2:1]#	1Tcyc-10		ns	1
	CDATA[15:0]				
t8e	Hold Time, CDATA[15:0] after IORD # High	0		ns	
	WAIT#				
t8f	Hold Time, IORD # Low after WAIT# High	1Tcyc+0		ns	1
t8g	Valid Delay, IORD # Low to WAIT# Low		50	ns	
	IOIS16#				
t8h	Valid Delay, CADR[25:0] to IOIS16# Low		50	ns	
	INPACK#				
t8k	Hold Time, INPCK# Low afterIORD# High	0		ns	
t8j	Valid Delay, IORD # Low to INPACK# Low		50	ns	

Note1: Tcyc is PCICLK cycle time.(Typically 30ns)
Note3: Tsu, Tpw, Thl can be programmed by setting 16-bit I/O Timing 0 register.



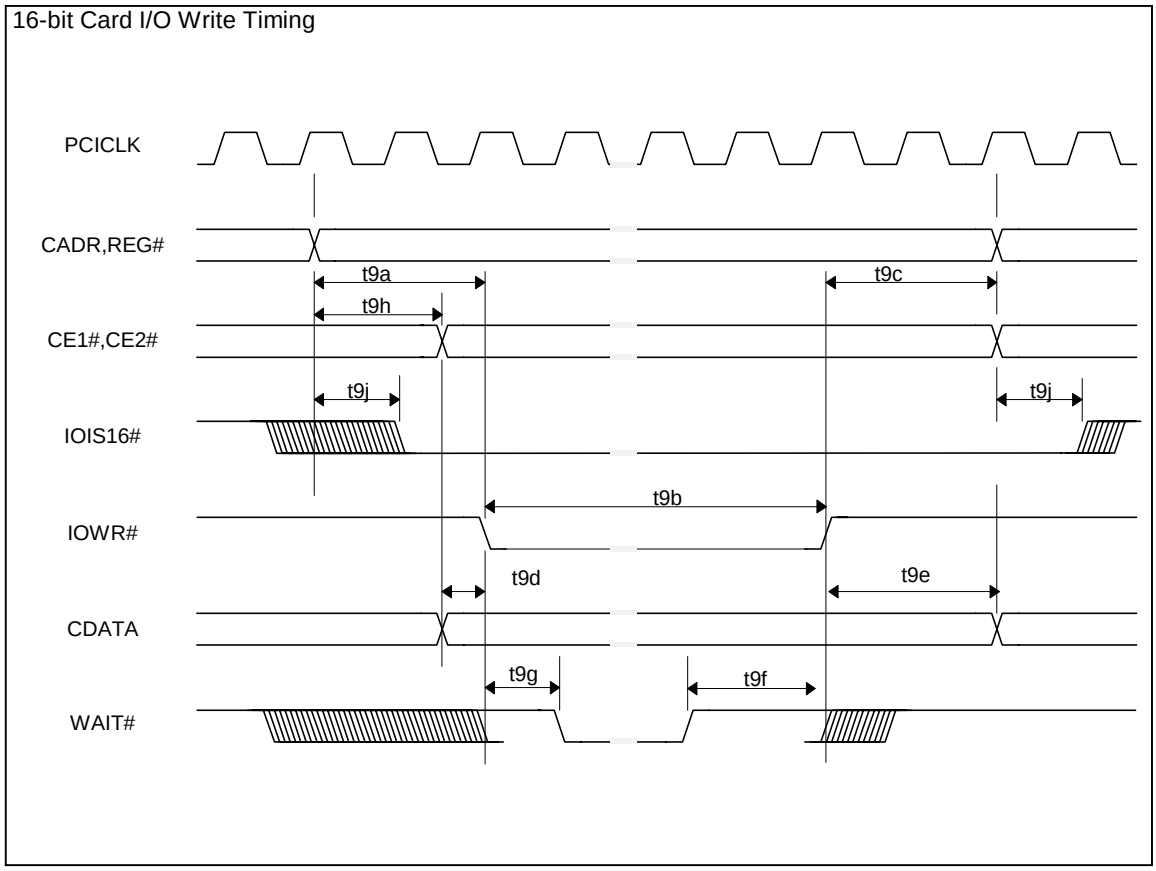
16-bit Card I/O Read Timing

I/O Write

(VCC_CORE=3.0~3.6V, VCC_SLOTA=3.0~3.6V or 4.75~5.25V, Ta=0~70˚C)

Symbol	Parameter	Min	Max	Unit	Notes
	CADR[25:0], REG#				
t9a	Setup Time, CADR[25:0] and REG# before IOWR # Low	Tsu-20		ns	1,3 Tsu=2~7Tcyc Programmable
t9c	Hold Time, CADR[25:0], REG# and CE[2:1]# after IOWR # High	Thl-10		ns	1,3 Thl=1~7Tcyc Programmable
	IOWR#				
t9b	Pulse Duration, IOWR# Low	Tpw-20		ns	1,3 Tpw=3~31Tcyc Programmable
	CE[2:1]#				
t9h	Valid Delay, CADR[15:0] and REG# to CE[2:1]#	1Tcyc-10		ns	1
	CDATA[15:0]				
t9d	Setup Time, CDATA[15:0] before IOWR # Low	Tsu-2Tcyc-10		ns	1,3 Tsu=3~7Tcyc Programmable
t9e	Hold Time, CDATA[15:0] after IOWR # High	Thl-10		ns	1,3 Thl=1~7Tcyc Programmable
	WAIT#				
t9f	Hold Time, IOWR # Low after WAIT# High	1Tcyc+0		ns	3
t9g	Valid Delay, IOWR # Low to WAIT# Low		50	ns	
	IOIS16#				
t9j	Valid Delay, CADR[25:0] and REG# to IOIS16# Low		50	ns	

Note1: Tcyc is PCICLK cycle time.(Typically 30ns)
Note3: Tsu, Tpw, Thl can be programmed by setting 16-bit I/O Timing 0 register.



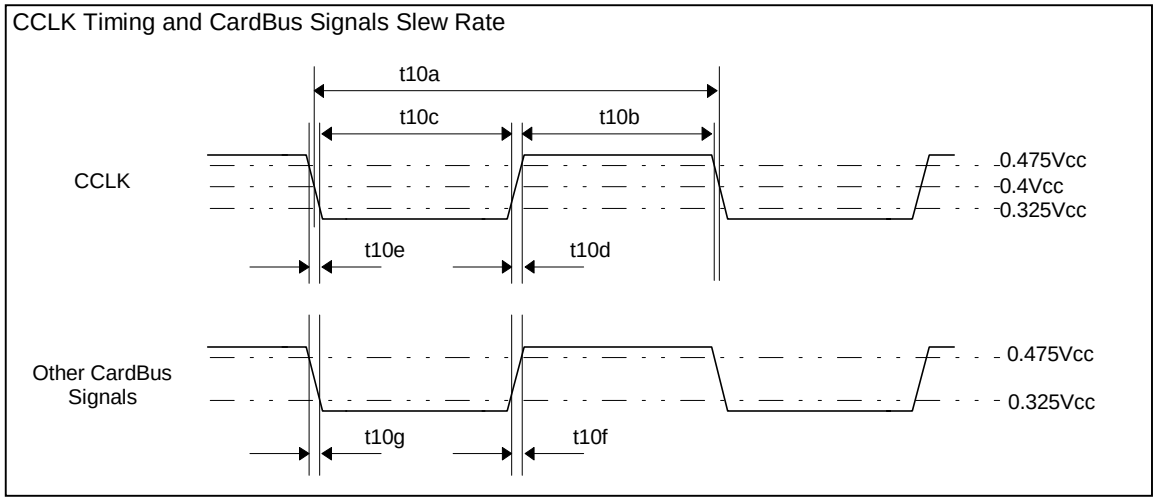
16-bit Card I/O Write Timing

8.3.4 CardBus PC Card Interface Signals

Clock and Signal Slew Rate

(VCC_CORE=3.0~3.6V, VCC_SLOTA=3.0~3.6V, Ta=0~70˚C)

Symbol	Parameter	Min	Max	Unit	Notes
	CCLK				
t10a	Cycle Time, CCLK	30		ns	
t10b	Pulse Width Duration, CCLK High	12		ns	
t10c	Pulse Width Duration, CCLK Low	12		ns	
t10d	Slew Rate, CCLK Rising Edge	1	4	V/ns	
t10e	Slew Rate, CCLK Falling Edge	1	4	V/ns	
	Other CardBus Signals				
t10f	Slew Rate, Rising Edge	0.25	1	V/ns	
t10g	Slew Rate, Falling Edge	0.25	1	V/ns	

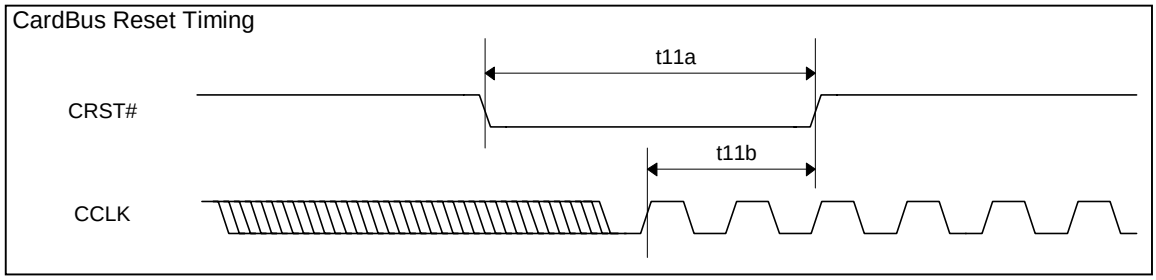


CCLK Timing and CardBus Slew Rate

Card Reset

(VCC_CORE=3.0~3.6V, VCC_SLOTA=3.0~3.6V, Ta=0~70˚C)

Symbol	Parameter	Min	Max	Unit	Notes
	CRST#				
t11a	Pulse Duration, CRST#	1		ms	
t11b	Setup Time,CCLK active at CRST# Negation	100		µs	

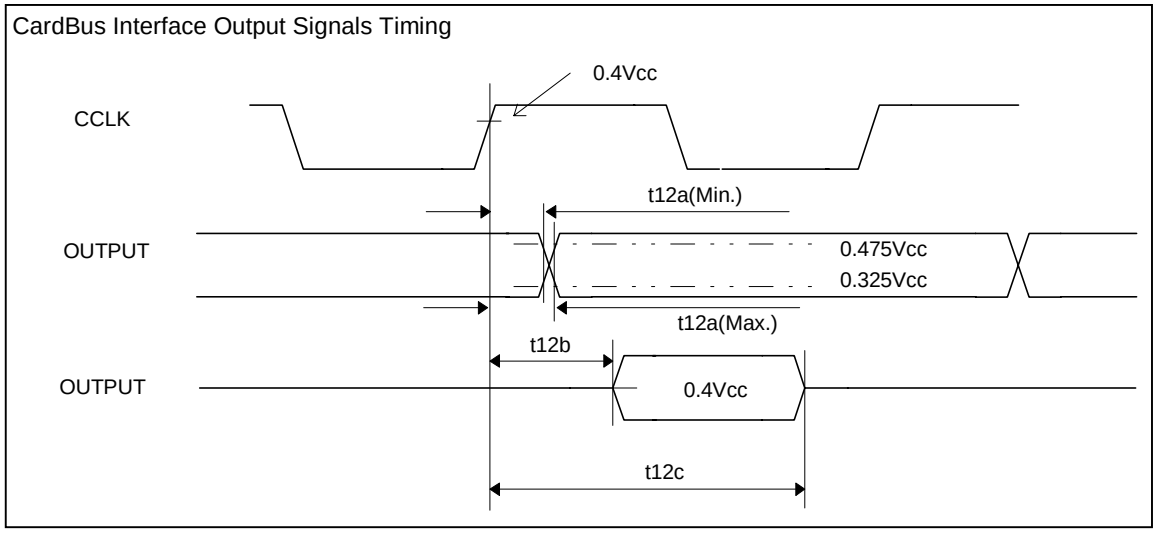


CardBus Reset Timing

Card Output

(VCC_CORE=3.0~3.6V, VCC_SLOTA=3.0~3.6V, Ta=0~70˚C)

Symbol	Parameter	Min	Max	Unit	Notes
	CAD[31:0], CC/BE#[3:0], CPAR, CFRAME#,CDEVSEL#, CIRDY#, CTRDY#,CSTOP#, CBLOCK#, CPERR#, CSERR#, CCLKRUN#, CGNT#				
t12a	Valid delay time from CCLK	2	18	ns	Min: CL=0 pF Max: CL=30 pF
t12b	Enable Time, Hi-Z to active delay from CCLK	2		ns	
t12c	Disable Time, Active to Hi-Z delay from CCLK		28	ns	

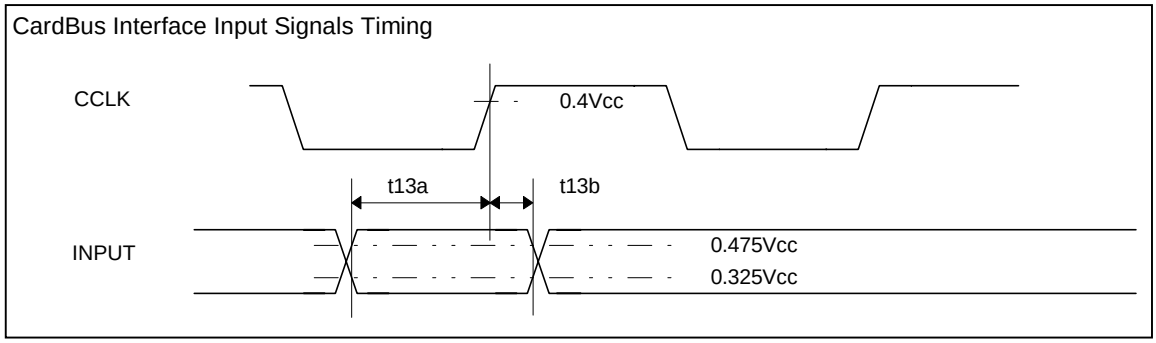


CardBus Interface Output Signals Timing

Card Input

(VCC_CORE=3.0~3.6V, VCC_SLOTA=3.0~3.6V, Ta=0~70˚C)

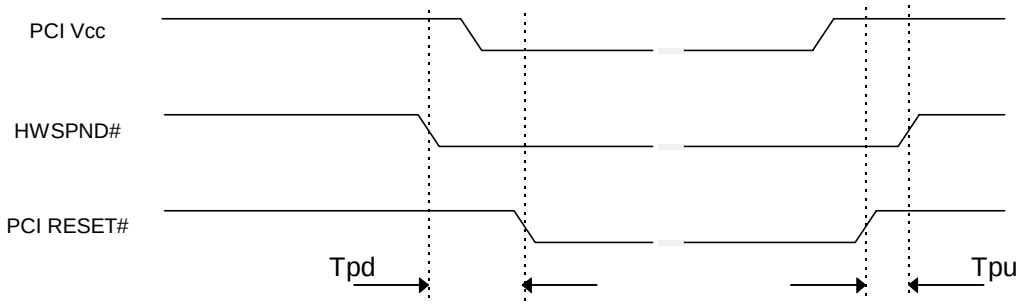
Symbol	Parameter	Min	Max	Unit	Notes
	CAD[31:0], CC/BE#[3:0], CPAR, CFRAME#,CDEVSEL#, CIRDY#, CTRDY#,CSTOP#, CBLOCK#, CPERR#, CSERR#, CCLKRUN#, CREQ#				
t13a	Setup Time, Signal Valid before CCLK	7		ns	
t13b	Hold Time, Signal Hold Time after CCLK High	0		ns	



CardBus Input Signals Timing

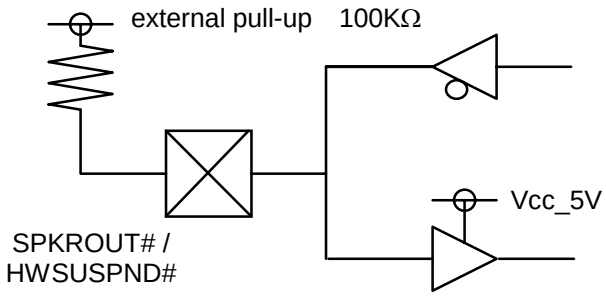
8.3.5 Hardware Suspend mode

Hardware Suspend Timing



Symbol	Parameter	Min	Typ	Max	Unit
Tpd	HWSPND# to PCIRESET# delay	100			ns
Tpu	HWSPND# to PCIRESET# delay	100			ns

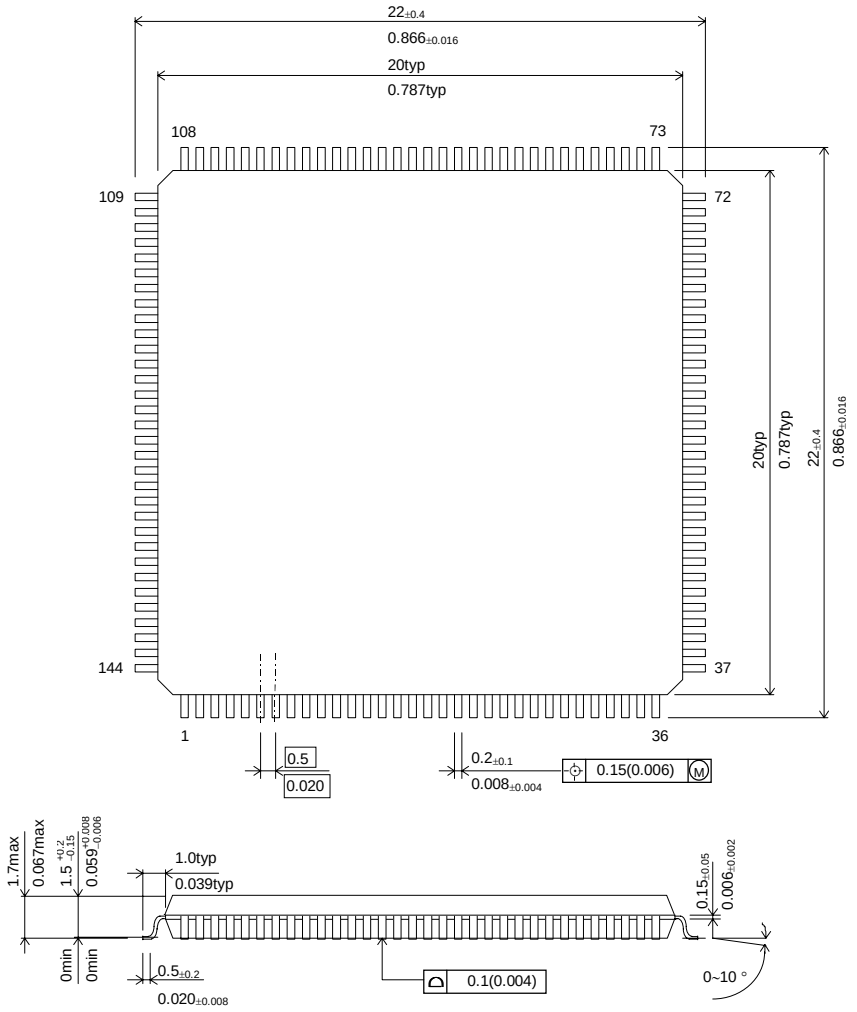
Hardware suspend Schematic



9 MECHANICAL PACKAGE OUTLINE

9.1 144pin LQFP

PACKAGE CODE	LQFP-144-P1(2020)



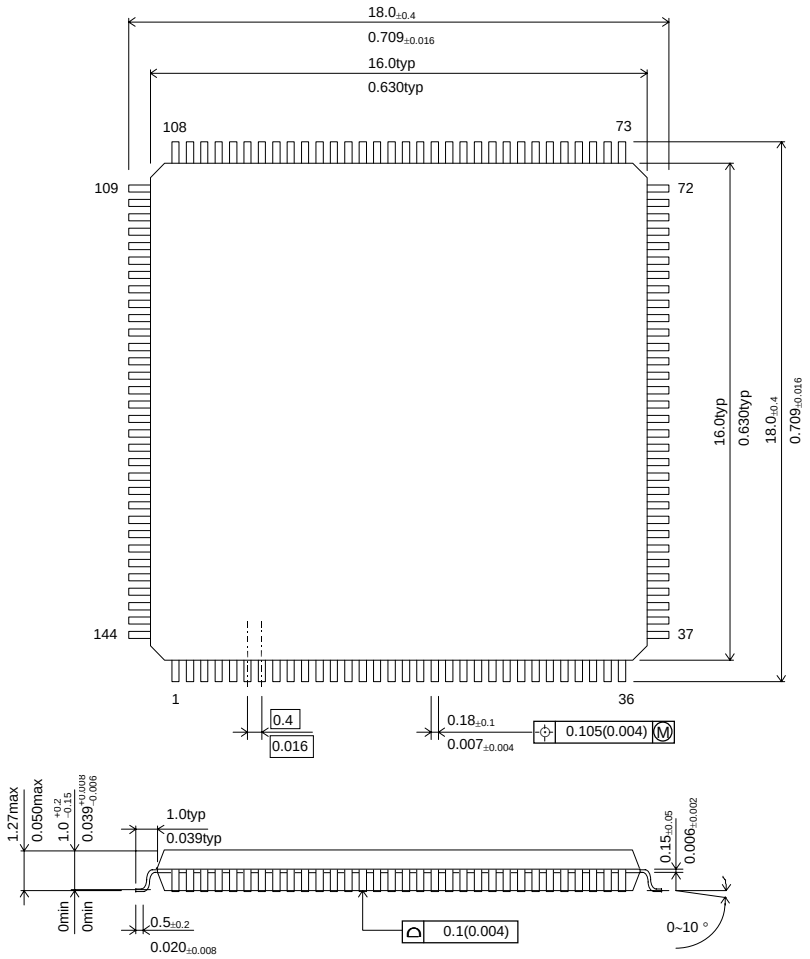
Reference

UNIT : MM / INCH

TITLE	LQFP-144PIN(P1) PACKAGE OUTLINE		
DATE	1998, 4, 21	PART NO.	DF-144LQFP-001(W)B
CHECKED	T.SEIGENJI	DRAWN	N.TAKEMURA

9.2 144pin TQFP

PACKAGE CODE	TQFP-144-P1(1616)



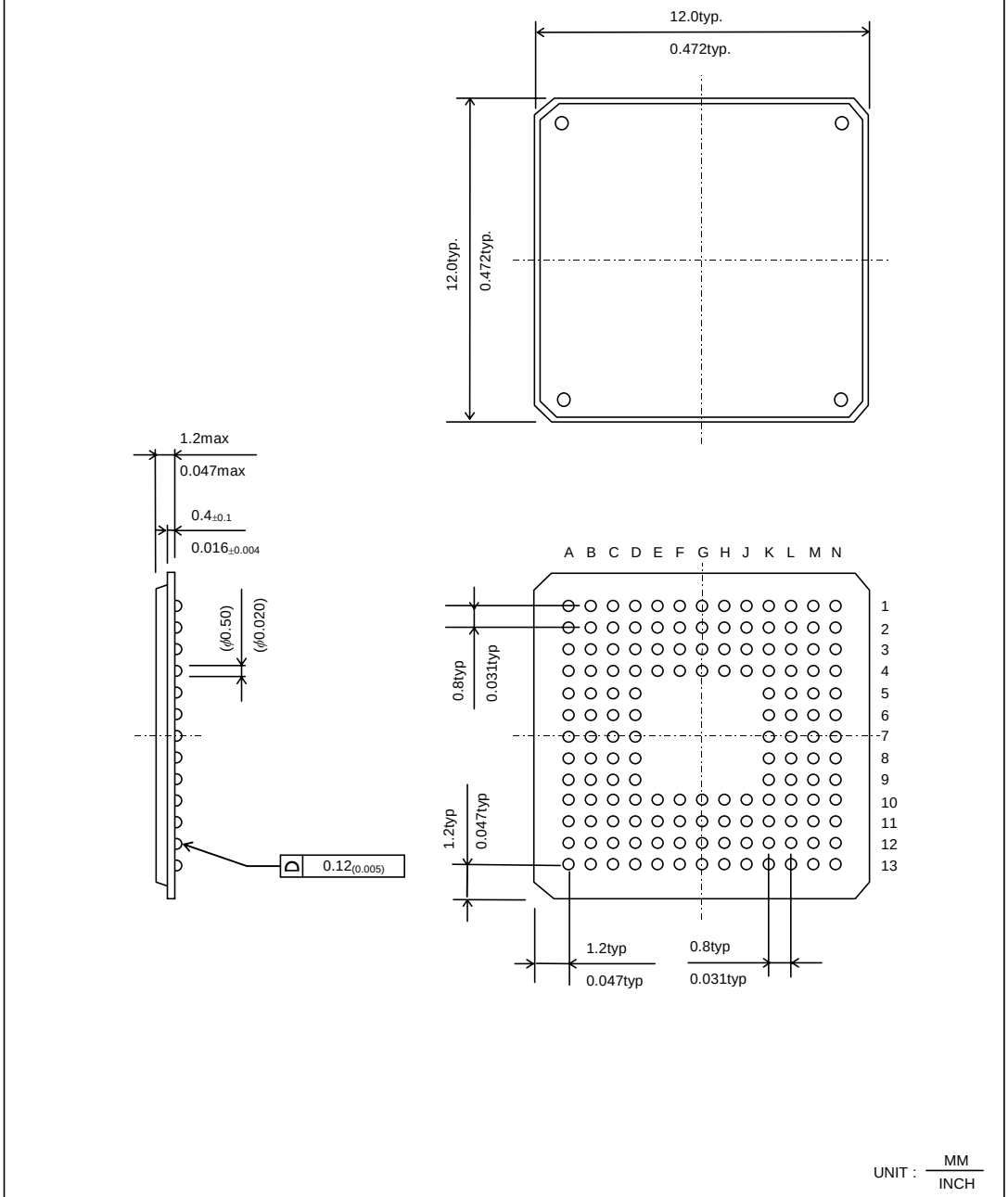
Reference

UNIT : MM / INCH

TITLE	TQFP-144PIN(P1) PACKAGE OUTLINE		
DATE	1998, 6, 23	PART NO.	DF-144TQFP-001(W)A
CHECKED	T.SEIGENJI	DRAWN	N.TAKEMURA

9.3 144pin CSP

PACKAGE CODE	CSP-144-P1(1212)



UNIT : MM / INCH

TITLE	CSP-144PIN(P1) PACKAGE OUTLINE		
DATE	1998, 6, 23	PART NO.	DF-144CSP-001(W)B
CHECKED	T.SEIGENJI	DRAWN	N.TAKEMURA

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