1045 Mission Court.
Fremont, CA 94539
USA
TEL: 1-510-683-3300 **FAX**: 1-510-683-3301

8th. Fl., No. 533
Chung-cheng Rd.,Hsin-tien
Taipei, Taiwan, R.O.C.
TEL: 886-2-218-5452 **FAX**: 886-2-218-5453

VIA VT83C465 PCMCIA SOCKET CONTROLLER

Date: March. 18, 1994

Overview

The VIA VT83C465 is a highly integrated PC Card socket controller chip implementing the PCMCIA 2.0/JEDIA 4.1 specifications. The chip is register compatible to the INTEL 82365SL, supporting two PC card sockets with fully buffered PCMCIA interface. No external buffer is required between the ISA bus and PCMCIA bus. For systems requiring more than two sockets, the VT83C465 can be cascaded to support up to four sockets without external logic.

In addition, the VT83C465 supports a jumperless configuration mechanism which allows the system manufacturer to support setup a configuration (CONFIG.SYS) driver for PC card setup.

Features

- Single chip PCMCIA controller between ISA bus and PCMCIA bus
- Full ExCA implementation of two PCMCIA 2.0/JEIDA 4.1 PC Card sockets
- Register-compatible with INTEL 82365SL
- Supports both memory cards and I/O cards
- Supports PCMCIA-ATA disk interface
- 8 or 16-bit CPU interface
- 8 or 16-bit PCMCIA interface support
- Cascadable up to four sockets without external logic
- High integration without any external logic or buffers
- Five mappable memory windows and two I/O windows for each socket
- Pin to Pin compatible with Cirrus Logic CL-PD6720
- 208 QFP/Two sockets support

Architectural Overview

The VT83C465 functional blocks include the PCMCIA/JEIDA PC Card socket interface, ISA interface, memory and I/O window mapping, socket power management features, interrupt steering, configuration registers and ATA mode operation.

PCMCIA/JEIDA PC Card Socket Interface

The PCMCIA/JEIDA interface consists of 60 signals and 8 power connections that interface to PC Cards through a 68 pin socket. A single VT83C465 can be configured to support either one or two sockets. Up to four PC Card sockets may be supported by cascading VT83C465 chips. This chip supports memory, I/O and ATA card interchangeably.

ISA Interface

The VT83C465 interfaces directly to the ISA bus. No external buffers or transceivers are needed. For systems based on the 386SL, this chip provides the special signals PWGOOD, SPKCSEL#, INTR# and RIOUT#.

Memory and I/O Window Mapping

Multiple PC cards in a system could conflict if they try to utilize the same system memory and I/O space. The VT83C465 allows the drivers to map memory card into up to five separate windows and I/O card into two separate windows, thus avoiding system configuration conflicts.
The VT83C465 provides memory paging, memory address mapping for both PC card attribute and common memory, and I/O address mapping. The VT83C465 includes registers which provide access to the card information structure and card configuration registers within PC card's attribute memory described by the PCMCIA/JEIDA PC Card Standard.

Socket Power Management

At power on, if there is no card plugged into any socket, power to the socket is turned off. When a card is inserted, one of two events occur. If the chip has been set for automatic power on, the VT83C465 automatically enables the power to socket. If the VT83C465 has been configured to cause management interrupts for card detection events, a management interrupt is generated to inform driver of the fact that a card was installed. Software driver can then initialize the card, or in the case of manual power detection, power the socket up manually and then initialize it.
When a card is removed from a socket, and if the VT83C465 has been configured for automatic power on, the VT83C465 automatically disables VCC and VPP supplies to the socket.

Interrupt Steering

The VT83C465 steers the interrupt from the PC card to one of ten system interrupts. Multiple PC cards in a system can conflict if they try to utilize the same interrupt level. The VT83C465 can be programmed to eliminate this conflict by steering each PC card interrupt request to a different system interrupt.

Configuration Registers

The VT83C465 provides a register containing interface identity and version information for each socket.

ATA Mode Operation

The VT83C465 supports direct connection to AT attached interface hard drives. ATA drives use an interface that is very similar to the IDE interface found on many popular portable computers. In this mode, the address and data conflict with the floppy drive is handled automatically.

PC Card interface I/O Register Addressing

The VT83C465 registers are accessed through an 8-bit indexing mechanism. Two I/O addresses are used to access the VT83C465 registers. The first I/O address is the index register, which is fixed at 3E0h. The second I/O address is the data register, which is fixed at 3E1h. Each VT83C465 contains a block of 64 indirectly access registers. The starting base of the index register values in each VT83C465 is selected by pull-up/pull-down strapping resistor on SPKCSEL# pin, according to the table below. While PWGOOD is false this pin becomes input. The rising edge of PWGOOD latches the pull up or down state of this pin, and thereafter this pin becomes normal operation. The VT83C465 will not respond to a data register read or write operation or to an index register read operation unless the index register has first been written to with a valid index.

SPKCSEL# Resistor	Base	Index	Data
Pull up	00h	3E0h	3E1h
Pull down	80h	3E0h	3E1h

Memory and I/O Mapping

The VT83C465 provides logic to map portions of the 64MB common memory and/or 64MB attribute memory spaces on the PC Card into the smaller 16MB (ISA) system address space. The VT83C465 mapping function provides extension of the system address space up to the full 64MB PC Card capability. Start and stop addresses are specified with ISA address bits 23 through 12. This sets the minimum size of a memory window into 4KB. Memory windows are specified in the ISA address from 64K to 16MB. Note that no memory window can be mapped in the first 64K of the ISA address space. Only I/O address windows are allowed to be mapped between 0 and 64KB in the ISA address space.

PC Card memory is access only when all of the following conditions are satisfied:

1. The system memory address mapping window is enabled.
2. The system memory address is greater than or equal to the system memory address mapping start register A23:A12.
3. The system memory address is less than or equal to the system memory address mapping stop register A23:A12..

An I/O PC Card is accessed when the following conditions are satisfied:

1. The I/O address window is enabled.
2. The system address is greater than or equal to the I/O address start register A15:A0.
3. The system address is less than or equal to the I/O address stop register A15:A0
4. The access is not a DMA transfer. AEN = 0 to access the I/O PC Card.

Register Set

The following is a list of VT83C465 registers and their offset values. The General Registers, Interrupt Registers, I/O Registers and Memory Registers are fully compatible with the Intel 82365SL. The other registers are unique to the VT83C465.

Socket A offset	Socket B offset	Register Name
00h	40h	Identification and Revision

01h	41h	Interface Status
02h	42h	Power and RESETDRV Control
03h	43h	Interrupt and General Control
04h	44h	Card Status Change
05h	45h	Card Status Change Interrupt Configuration
06h	46h	Address Window Enable
07h	47h	I/O Control
08h	48h	I/O Address 0 Start Low Byte
09h	49h	I/O Address 0 Start High Byte
0Ah	4Ah	I/O Address 0 Stop Low Byte
0Bh	4Bh	I/O Address 0 Stop High Byte
0Ch	4Ch	I/O Address 1 Start Low Byte
0Dh	4Dh	I/O Address 1 Start High Byte
0Eh	4Eh	I/O Address 1 Stop Low Byte
0Fh	4Fh	I/O Address 1 Stop High Byte
10h	50h	System Memory Address 0 Mapping Start Low Byte
11h	51h	System Memory Address 0 Mapping Start High Byte
12h	52h	System Memory Address 0 Mapping Stop Low Byte
13h	53h	System Memory Address 0 Mapping Stop High Byte
14h	54h	Card Memory Offset Address 0 Low Byte
15h	55h	Card Memory Offset Address 0 High Byte
16h	56h	Misc Control 1
17h	57h	Reserved
18h	58h	System Memory Address 1 Mapping Start Low Byte
19h	59h	System Memory Address 1 Mapping Start High Byte
1Ah	5Ah	System Memory Address 1 Mapping Stop Low Byte
1Bh	5Bh	System Memory Address 1 Mapping Stop High Byte
1Ch	5Ch	Card Memory Offset Address 1 Low Byte
1Dh	5Dh	Card Memory Offset Address 1 High Byte
1Eh	5Eh	Misc Control 2
1Fh	5Fh	Chip Information
20h	60h	System Memory Address 2 Mapping Start Low Byte
21h	61h	System Memory Address 2 Mapping Start High Byte
22h	62h	System Memory Address 2 Mapping Stop Low Byte
23h	63h	System Memory Address 2 Mapping Stop High Byte
24h	64h	Card Memory Offset Address 2 Low Byte
25h	65h	Card Memory Offset Address 2 High Byte
26h	66h	ATA Mode Control
27h	67h	Reserved
28h	68h	System Memory Address 3 Mapping Start Low Byte
29h	69h	System Memory Address 3 Mapping Start High Byte

Socket A offset	Socket B offset	Register Name
2Ah	6Ah	System Memory Address 3 Mapping Stop Low Byte
2Bh	6Bh	System Memory Address 3 Mapping Stop High Byte

2Ch	6Ch	Card Memory Offset Address 3 Low Byte
2Dh	6Dh	Card Memory Offset Address 3 High Byte
2Eh	6Eh	Reserved
2Fh	6Fh	Reserved
30h	70h	System Memory Address 4 Mapping Start Low Byte
31h	71h	System Memory Address 4 Mapping Start High Byte
32h	72h	System Memory Address 4 Mapping Stop Low Byte
33h	73h	System Memory Address 4 Mapping Stop High Byte
34h	74h	Card Memory Offset Address 4 Low Byte
35h	75h	Card Memory Offset Address 4 High Byte
36h	76h	Reserved
37h	77h	Reserved
38h	78h	Reserved
39h	79h	Reserved
4Ah	7Ah	Reserved
4Bh	7Bh	Reserved
4Ch	7Ch	Reserved
4Dh	7Dh	Reserved
4Eh	7Eh	Reserved
4Fh	7Fh	Reserved

Chip Control Registers

Identification and Revision Register (Read Only)
Address : Index (Base + 00h)

Bit	Function
D[7:6]	VT83C465 Interface Type Type of PC Card supported by the socket. These bits do not identify the type of card that is present at the socket. 00: I/O only. 01: Memory only. 10: Memory & I/O. 11: Reserved.
D[5:4]	Reserved. These bits will be read back as zero.
D[3:0]	These four bits indicate the revision of the chip. 0010 is compatible with Intel.

Interface Status Register (Read Only)
Address : Index (Base + 01h)

Bit	Function

D7	Vpp_Valid. Indicates the state of the Vpp_Valid# pin. 0: is inactive. 1: is active.
D6	PC Card Power Active 0: Power to the socket is off (Vcc and Vpp1 are no connection). 1: Power to the socket is on (Vcc = 5V and Vpp1 is set according to bit 1:0 in the power control register).
D5	Ready/Busy# 0: PC Card is busy. 1: PC Card is ready.
D4	Memory Write Protect. Bit value is the logic level of the WP signal on the memory PC Card interface. 0: PC Card is not write protected. 1: PC Card is write protected.
D3	Card Detect 2 Together with card detect 1 indicates a card is present at the socket and fully seated. 0: CD2# signal on the PC Card interface is inactive. 1: CD2# signal on the PC Cars interface is active.
D2	Card Detect 1 Together with card detect 2 indicates a card is present at the socket and fully seated. 0: CD1# signal on the PC Card interface is inactive. 1: CD1# signal on the PC Cars interface is active.
D[1:0]	Battery Voltage Detect 2 and 1. BVD1 BVD2 Status 0 0 battery dead 0 1 battery dead 1 0 warning 1 1 battery good For I/O PC Cards, bit 0 indicates the current status of the (STSCHG/RI#) signal from the PC Card when the ring indicate enable bit in the Interrupt and General control register is set to 0.

Power and RESETDRV Control Register (Read/Write)
Address : Index (Base + 02h)

Bit	Function

D7	Output Enable. If this bit set to zero, the PC Card outputs listed below are tri-stated. CADR<25:0>, D<15:0>, CE2#, CE1#, IORD#, IOWR#, OE#, WE#, REG#, RESET. This bit should not be set until after this register has been written setting PC Card Power Enable previously.
D6	Disable Resume RESETDRV. Not support.
D5	Auto Power Switch Enable. 0: automatic socket power switching based on card detects is disable. 1: automatic socket power switching based on card detects is enable.
D4	PC Card Power Enable. 0: power to the socket is disabled. (Vcc and Vpp1 are all no connection) 1: power to the socket is enabled. (Vcc = 5V and Vpp1 is set according to bit 1:0 in this register)
D[3:2]	R/W:00
D[1:0]	Vpp1 Power Control 00: no connection. 01: Vcc. 10: Vpp. 11: reserved.(this setting then Vpp1 will be a no connection)

The following table describes the slot power control function.

Output	PC Card Power Enable	Auto Power Switch Enable	CD1#	CD2#	Tri-state Outputs	PC Card Power Active
x	0	x	x	x	OFF	0
0	1	0	0	0	OFF	1
1	1	0	0	0	ON	1
x	1	0	x	1	OFF	1
x	1	0	1	x	OFF	1
0	1	1	0	0	OFF	1
1	1	1	0	0	ON	1
x	1	1	x	1	OFF	0
x	1	1	1	x	OFF	0

Interrupt Register (Read/Write)
Address : Index (Base + 03h)

Bit	Function

D7	Ring Indicate Enable. 0: For I/O PC Card, the STSCHG/RI# signal from card is used as the status change signal STSCHG#. The current status of this signal is then available to be read from the interrupt status register and this signal can be configured as a source for the card status change interrupt. 1: For I/O PC Card, the STSCHG/RI# signal from card is used as ring indicator signal and is passed through to the IRQ15(multi pin, set Misc Control 2 bit 7 to one is used as RI_OUT#). The ring indicate enable bit has no function when the PC Card type bit is set to zero (memory card).
D6	PC Card Reset This is a software reset to PC Card. 0: Activates the RESET to the PC Card. The RESET signal will be active until bit is set to one. 1: Deactivates the RESET signal to the PC Card.
D5	PC Card Type. 0: Memory PC Card. 1: I/O PC Card.
D4	INTR# Enable. 0: The INTR# does not indicate a card status change interrupt is steered to one of the IRQs lines according to bit 7:4 in the card status change interrupt configuration register. 1: Enable the card status change interrupt on the INTR# signal.
D[3:0]	IRQ Level Selection (I/O Cards Only). Refer to following table is the redirection of the PC Card interrupt according to these bits.

IRQ bit3	IRQ bit2	IRQ bit1	IRQ bit0	Interrupt Request Level
0	0	0	0	IRQ not select
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	IRQ3 enable
0	1	0	0	IRQ4 enable
0	1	0	1	IRQ5 enable
0	1	1	0	Reserved
0	1	1	1	IRQ7 enable
1	0	0	0	Reserved
1	0	0	1	IRQ9 enable
1	0	1	0	IRQ10 enable
1	0	1	1	IRQ11 enable
1	1	0	0	IRQ12 enable
1	1	0	1	Reserved
1	1	1	0	IRQ14 enable
1	1	1	1	IRQ15 enable

Card Status Change Register (Read Only)
Address : Index (Base + 04h)

Bit	Function
D[7:4]	R. 0000

D3	Card Detect Change. 0: No change detected on either CD2# or CD1#. 1: A change has been detected on CD2# and CD1#.
D2	Ready Change. 0: No change on RDY/BSY#, or I/O PC Card installed. 1: When a low to high has been detected on the RDY/BSY# signal indicating that the memory PC Card is ready to accept a new data transfer.
D1	Battery Warning. 0: No battery warning condition, or I/O PC Card installed. 1: A battery warning condition has been detected.
D0	Battery Dead (STSCHG#) For memory PC Cards, bit is set one when a battery dead condition has been detected. For I/O PC Cards, bit is set to one if ring indicate enable bit in the interrupt and general control register is set to zero and the STSCHG/RI# signal from the I/O PC Card has been pulled low. The system software then has to read the status change register in the PC Card to determine the cause of the status change signal STSCHG#. This bit reads zero for I/O PC Cards if the ring indicate enable bit in the interrupt and general control register is set to one.

NOTE : The Card Status Change Register contains the status for sources of the card status change interrupt. These sources can be enabled to generate a card status change interrupt by setting the corresponding bit in the card status change interrupt configuration register. Reading the Card Status Change Register causes the register bits to be reset to zero.
If the card status change interrupt is enabled to one of the system bus interrupt request lines, the corresponding IRQ signal remains active high until this register is read.

Card Status Change Interrupt Configuration Register (Read/Write)
Address : Index (Base + 05h)

Bit	Function
D[7:4]	Interrupt Steering for the Card Status Change Interrupt. These bits select the redirection of the card status change interrupt if the interrupt is not select to the output on the INTR# pin.
D3	Card Detect Enable. 0: Disables the generation of a card status change interrupt when the card detect signals changed. 1: Enables a card status change interrupt when a change has been detected on CD2# or CD1#.
D2	Ready Enable (Memory Card Only). 0: Disables the generation of a card status change interrupt when a low to high transition has been detected on the RDY/BSY# signal. 1: Enables a card status change interrupt when a low to high transition has been detected on the RDY/BSY# pin.
D1	Battery Warning Enable (Memory Card Only). 0: Disables the generation of a card status change interrupt when a battery warning condition has been detected. 1: Enables a card status change interrupt when a battery warning condition has been detected.
D0	Battery Dead Enable (STSCHG#). 0: Disables the generation of a card status change interrupt when a battery dead condition has been detected. (Memory PC Cards used). For I/O PC Cards, bit is ignored when a Ring Indicate Enable bit is set one. 1: For memory PC Cards, enables a card status change interrupt when a battery dead condition has been detected. For I/O PC Cards, enables the VT83C465 to generate a card status change interrupt if the STSCHG# signal has been pulled low by the I/O PC Card, assuming that the Ring Indicate Enable bit is set zero.

INTR Enable	IRQ bit3	IRQ bit2	IRQ bit1	IRQ bit0	Interrupt Request Level
0	0	0	0	0	IRQ not select
0	0	0	0	1	Reserved
0	0	0	1	0	Reserved
0	0	0	1	1	IRQ3 enable
0	0	1	0	0	IRQ4 enable
0	0	1	0	1	IRQ5 enable
0	0	1	1	0	Reserved
0	0	1	1	1	IRQ7 enable
0	1	0	0	0	Reserved
0	1	0	0	1	IRQ9 enable
0	1	0	1	0	IRQ10 enable
0	1	0	1	1	IRQ11 enable
0	1	1	0	0	IRQ12 enable
0	1	1	0	1	Reserved
0	1	1	1	0	IRQ14 enable
0	1	1	1	1	IRQ15 enable
1	x	x	x	x	Card Status Change Interrupt on INTR#

Address Window Enable Register (Read/Write)
Address : Index (Base + 06h)

Bit	Function
D[7:6]	I/O Window Enable [1:0]. 0: Inhibit the card enable signals to the PC Card when an I/O access occurs within the corresponding I/O address window. 1: Generate the card enable signals to PC card when an I/O access occurs within the corresponding I/O address window. I/O accesses pass addresses from the system bus directly through to the PC Card. The start and stop register pairs must all be set to the desired window values before setting this bit to one.
D5	MS16# Decode A23:12. 0: Generated MS16# from a decode of the system address lines A23:17 only. This means that a minimum, a 128K block of system memory address space is set aside as 16-bit memory only. 1: Generated MS16# from a decode of the system address lines A23:12.
D4	Memory Window 4 Enable. 0: Inhibit the card enable signals to the PC Card when a memory access occurs within the corresponding system memory address window. 1: Generate the card enable signals when a memory access occurs within the corresponding system memory address window. When the system address is within the window, the computed address will be generated to the PC Card.
D3	Memory Window 3 Enable. 0: Inhibit the card enable signals to the PC Card when a memory access occurs within the corresponding system memory address window. 1: Generate the card enable signals when a memory access occurs within the corresponding system memory address window. When the system address is within the window, the computed address will be generated to the PC Card.
D2	Memory Window 2 Enable. 0: Inhibit the card enable signals to the PC Card when a memory access occurs within the corresponding system memory address window. 1: Generate the card enable signals when a memory access occurs within the corresponding system memory address window. When the system address is within the window, the computed address will be generated to the PC Card.
D1	Memory Window 1 Enable. 0: Inhibit the card enable signals to the PC Card when a memory access occurs within the corresponding system memory address window. 1: Generate the card enable signals when a memory access occurs within the corresponding system memory address window. When the system address is within the window, the computed address will be generated to the PC Card.
D0	Memory Window 0 Enable. 0: Inhibit the card enable signals to the PC Card when a memory access occurs within the corresponding system memory address window. 1: Generate the card enable signals when a memory access occurs within the corresponding system memory address window. When the system address is within the window, the computed address will be generated to the PC Card. NOTE: The start, stop and offset registers pairs must all be set to the desired window values before setting bit to one.(All Memory Windows).

I/O Control Register (Read/Write)
Address : Index (Base + 07h)

Bit	Function
D7	I/O Window 1 Wait State. 0: 16-bit system accesses occur with no additional wait state. 1: 16-bit system accesses occur with one additional wait state(4 BUSCLKs).
D6	I/O Window 1 zero wait state. 0: 8-bit system I/O access will occur with additional wait state. 1: 8-bit system I/O access will occur with no additional wait state and the NOWS# will be returned to the system bus.
D5	I/O Window 1 IOCS16# Source. 0: IOCS16# is generated based on the value of the data size bit. 1: IOCS16# is generated based on the IOIS16# signal from PC Card.
D4	I/O Window 1 Data Size. 0: 8-bit I/O data path to PC Card. 1: 16-bit I/O data path to PC Card.
D3	I/O Window 0 Wait State. 0: 16-bit system accesses occur with no additional wait state. 1: 16-bit system accesses occur with one additional wait state(4 BUSCLKs).
D2	I/O Window 0 zero wait state. 0: 8-bit system I/O access will occur with additional wait state. 1: 8-bit system I/O access will occur with no additional wait state and the NOWS# will be returned to the system bus.
D1	I/O Window 0 IOCS16# Source. 0: IOCS16# is generated based on the value of the data size bit. 1: IOCS16# is generated based on the IOIS16# signal from PC Card.
D0	I/O Window 0 Data Size. 0: 8-bit I/O data path to PC Card. 1: 16-bit I/O data path to PC Card.

I/O Address Start Register Low Byte (Read/Write)
Address : Window 0 Index (Base + 08h)
Address : Window 1 Index (Base + 0Ch)

Bit	Function
D[7:0]	I/O Window Start Address A[7:0] Low order address bits used to determine the start address of the corresponding I/O address window. This provides a minimum 1 byte window for I/O address window.

I/O Address Start Register High Byte (Read/Write)
Address : Window 0 Index (Base + 09h)
Address : Window 1 Index (Base + 0Dh)

Bit	Function
D[7:0]	I/O Window Start Address A[15:8] High order address bits used to determine the start address of the corresponding I/O address window.

I/O Address Stop Register Low Byte (Read/Write)
Address : Window 0 Index (Base + 0Ah)
Address : Window 1 Index (Base + 0Eh)

Bit	Function
D[7:0]	I/O Window Stop Address A[7:0] Low order address bits used to determine the stop address of the corresponding I/O address window. This provides a minimum 1 byte window for I/O address window.

I/O Address Stop Register High Byte (Read/Write)
Address : Window 0 Index (Base + 0Bh)
Address : Window 1 Index (Base + 0Fh)

Bit	Function
D[7:0]	I/O Window Stop Address A[15:8] High order address bits used to determine the stop address of the corresponding I/O address window.

System Memory Address Mapping Start Low Byte Register (Read/Write)
Address : Window 0 Index (Base + 10h)
Address : Window 1 Index (Base + 18h)
Address : Window 2 Index (Base + 20h)
Address : Window 3 Index (Base + 28h)
Address : Window 4 Index (Base + 30h)

Bit	Function
D[7:0]	System Memory Window Start Address A[19:12] Low order address bits used to determine the start address of the corresponding system memory address mapping window. This provides a minimum 4K bytes window for memory address mapping window.

System Memory Address Mapping Start High Byte Register (Read/Write)
Address : Window 0 Index (Base + 11h)
Address : Window 1 Index (Base + 19h)
Address : Window 2 Index (Base + 21h)
Address : Window 3 Index (Base + 29h)
Address : Window 4 Index (Base + 31h)

Bit	Function
D7	Data Size. 0: 8-bit memory data path to the PC Card. 1: 16-bit memory data path to the PC Card.
D6	Zero Wait State. 0: System memory access will occur with additional wait states. 1: System memory access will occur with no additional wait states and the NOWS# signal will be returned to the system bus. The WAIT# signal from PC Card will override this bit.
D[5:4]	R/W. 00
D[3:0]	System Memory Window Start Address A23:20. High order address bits used to determine the start address of the corresponding system memory address mapping window.

System Memory Address Mapping Stop Low Byte Register (Read/Write)
Address : Window 0 Index (Base + 12h)
Address : Window 1 Index (Base + 1Ah)
Address : Window 2 Index (Base + 22h)

Address : Window 3 Index (Base + 2Ah)
Address : Window 4 Index (Base + 32h)

Bit	Function
D[7:0]	System Memory Window Stop Address A[19:12] Low order address bits used to determine the stop address of the corresponding system memory address mapping window. This provides a minimum 4K bytes window for memory address mapping window.

System Memory Address Mapping Start High Byte Register (Read/Write)
Address : Window 0 Index (Base + 13h)
Address : Window 1 Index (Base + 1Bh)
Address : Window 2 Index (Base + 23h)
Address : Window 3 Index (Base + 2Bh)
Address : Window 4 Index (Base + 33h)

Bit	Function
D[7:6]	Wait State bit 1:0. These bits determine the number of additional wait states for a 16-bit access to the system memory window. If the PC Card supports the WAIT# signal, wait states will be generated by the PC Card asserting the WAIT# signal. 00: standard 16-bit cycle (3 BUSCLKs per access) 01: 1 additional wait state (4 BUSCLKs per access) 10: 2 additional wait states (5 BUSCLKs per access) 11: 3 additional wait states (6 BUSCLKs per access)
D[5:4]	R/W. 00
D[3:0]	System Memory Window Stop Address A23:20. High order address bits used to determine the stop address of the corresponding system memory window.

System Memory Address Mapping Offset Low Byte Register (Read/Write)
Address : Window 0 Index (Base + 14h)
Address : Window 1 Index (Base + 1Ch)
Address : Window 2 Index (Base + 24h)
Address : Window 3 Index (Base + 2Ch)
Address : Window 4 Index (Base + 34h)

Bit	Function
D[7:0]	System Memory Window Offset Address A[19:12] Low order address bits which added to the system address bits A19:12 to generate card address.

System Memory Address Mapping Offset High Byte Register (Read/Write)
Address : Window 0 Index (Base + 15h)
Address : Window 1 Index (Base + 1Dh)
Address : Window 2 Index (Base + 25h)
Address : Window 3 Index (Base + 2Dh)
Address : Window 4 Index (Base + 35h)

Bit	Function
D7	Write Protect. 0: Write operations to PC Card through the corresponding system memory window are allowed. 1: Write operations to PC Card through the corresponding system memory window are inhibited.
D6	REG Active. 0: Access to the system memory will result in common memory space. 1: Access to the system memory will result in attribute memory space.
D[5:0]	Card Memory Offset Address A25:20. High order address bits which are added to the system address A23:20 to generate card address.

Extension Registers

Misc. Control 1 Register (Read/Write)
Address : Index (Base + 16h)

Bit	Function
D7	Inpack Support. 0: Inpack not support. 1: Inpack used to control data bus drivers during I/O read from the PC Card.
D[6:5]	R/W. 00
D4	Speaker Enable. 0: SPKCSEL# is tri-state. 1: SPKCSEL# is driven form the XOR of SPKR# from each enabled PC Card.
D[3:0]	R/W. 0000

Misc. Control 2 Register (Read/Write)
Address : Index (Base + 1Eh)

Bit	Function
D7	IRQ15 is RI Out. This bit determines the function of the IRQ15. When configured for ring indicate, IRQ15 is used to resume the 386SL when a high to low change is detected on the STSCHG#. 0: Normal IRQ15 operation. 1: IRQ15 is connected to Ring Indicate on the processor.
D6	R/W. 0
D5	Tri-state SD7 bit. This bit enables floppy change bit compatibility. 0: Normal operation. 1: For I/O PC Card at address 03F7h and 0377h, do not drive SD7 bit.

D4	Drive LED Enable. This bit determines when SPKR# is used to drive an LED on IRQ12 for disk access. 0: Normal IRQ12 operation. 1: IRQ12 becomes an open drain output suitable for driving an LED.
D[3:0]	R/W. 0000

Compatible Chip Information with Cirrus Logic CL-6720 Register (Read/Write)
Address : Index (Base + 1Fh)

Bit	Function
D[7:6]	Chip Identification. (Read Only) This field identifies the VT83C465 device and compatible with Cirrus Logic CL-6720 device. For the first read of this register this field will be 11h; on the next read will be 00h.
D5	Dual/Single Socket. (Read Only) This bit will be 1b, because the VT83C465 is support two sockets.
D[4:2]	VT83C465 Revision. (Read Only) This field identifies the revision of this controller. It's initial value is 111h.
D[1:0]	R/W. 00

ATA Mode Control Register (Read/Write)
Address : Index (Base + 26h)

Bit	Function
D7	A25/CSEL. In ATA mode, this bit is applied to the ATA A25/CSEL and is vendor specific. Certain ATA drive vendor specific performance enhancements beyond the PCMCIA 2.0 standard may be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.
D6	A24/M/S#. In ATA mode, this bit is applied to the ATA A24/M/S# and is vendor specific. Certain ATA drive vendor specific performance enhancements beyond the PCMCIA 2.0 standard may be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.
D5	A23/VU. In ATA mode, this bit is applied to the ATA A23/VU and is vendor specific. Certain ATA drive vendor specific performance enhancements beyond the PCMCIA 2.0 standard may be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.
D4	A22. In ATA mode, this bit is applied to the ATA A22 and is vendor specific. Certain ATA drive vendor specific performance enhancements beyond the PCMCIA 2.0 standard may be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.
9D3	A21. In ATA mode, this bit is applied to the ATA A21 and is vendor specific. Certain ATA drive vendor specific performance enhancements beyond the PCMCIA 2.0 standard may be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.
D2	R/W. 0
D1	Speaker is LED Input. 0: Normal operation. 1: The PC Card SPKR# pin will be used to drive IRQ12 if Drive LED Enable is set.

D0	ATA Mode. 0: Normal operation. 1: Configures the socket interface to handle ATA type III disk drives.

VT83C465 Pin Description

Signal	Description	Pin	Type	Drive
ISA Bus Interface				
A0:A23	Address Bus : Lines driven by the host system that enable direct addressing of up to 16Mbytes of memory on a card. In a 16-bit ISA system, A<23:17> should be connected to LA<23:17> and A<16:0> should be connected to SA<16:0>.	157,155,153,151,149,147,146,184,183,182,181,179,178,176,175,173,171,169,168,167,165,164,162,161	I	N/A
SD0:SD15	CPU Data I/O : These pins are used to transfer data during a memory or I/O cycle.	134,135,136,137,139,141,142,143,200,199,197,196,194,193,190,189	B	12ma
AEN	System Address Enable	187	I	N/A
BALE	Address Latch Enable : This active high is used to latch A23:A17 bus lines.	166	I	N/A
INTR#	Interrupt : This signal indicates a management interrupt. This should be connected to either SMI or NMI depending on the type of CPU used.	203	O	4ma
SBHE	System Bus High Enable : When this signal is low, it indicates that data is valid on the upper byte of the 16-bit data bus.	159	I	N/A
IOCHRDY#	I/O Channel Ready : This signal is driven low to lengthen host cycles.	188	TO	12ma
IOCS16#	16-bit I/O Transfer Mode Chip Select : This signal is used by the host system to determine when a 16-bit or 8-bit conversion is needed for CPU accesses. A 16 to 8 conversion is done anytime the System bus controller requests a 16-bit I/O cycle and IOCS16# is sampled high.	158	TO	12ma
IOR#	I/O Port Read : This indicates that a host I/O read cycle is taking place.	185	I	N/A
IOW#	I/O Port Write : This indicates that a host I/O write cycle is taking place.	186	I	N/A
MS16#	16-bit Memory Transfer Mode Chip Select : This signal is used by the host system to determine when a 16-bit or 8-bit conversion is needed for CPU accesses. A 16 to 8 conversion is done anytime the System bus controller requests a 16-bit memory cycle and MS16# is sampled high.	160	TO	12ma
MEMR#	System Memory Read : Active low signal indicates a read cycle.	145	I	N/A
MEMW#	System Memory Write : Active low signal indicates a write cycle.	144	I	N/A

NOWS#	Zero Wait State : This active low indicates that a PC Card wishes to execute an 8-bit zero wait state bus cycle. This signal will not be driven during a 16-bit access.	191	TO	12ma
PWGOOD	Power Good : Active high signal indicates the power to the system is stable.	201	I	N/A
IRQ14,11-9,7,5-3	System Interrupt Request : These active high signals are used to request interrupt service.	148,154,156,198,177,174,172,170	TO	4ma
IRQ15	System Interrupt Request 15 : In IRQ mode this is signal indicates an interrupt request. When IRQ15 is RI_OUT, this pin is used to resume the CPU using RI pin of the 80386SL set.	150	TO	4ma
IRQ12	System Interrupt Request 12 : In IRQ mode this is signal indicates an interrupt request. When LED Drive Enable is set to 1, this signal becomes an open drain driver for disk active LED.	152	TO	4ma
BCLK	Bus Clock	163	I	N/A
PC Card Interface				
VPPVLD#	Vpp Valid : This active low indicates the Vpp power lines have reached the user specified range.	3	I	N/A
ISA_VCC	Host Bus Vcc Pin : The ISA interface pin are applied to +5V.	138,195	I	N/A
A_BVD1, A_BVD2, B_BVD1, B_BVD2 (STSCHG/RI) (SPKR#)	Battery Voltage Detect : Generated by memory PC Card that include batteries. The signals are an indication of the condition of the battery on the memory PC Card. Both BVD1 and BVD2 are kept asserted high when the battery is in good condition. When BVD2 is negated while BVD1 is still asserted, the battery is in warning condition and should be replaced. If BVD1 is negated with BVD2 either asserted or negated, the battery is no longer serviceable and data is lost. Status Change : In I/O mode ,it will be STSCHG input, which indicates that the status of the card has changed. Ring Indicate : Signal is qualified by the Ring Indicate Enable bit (Interrupt and General control Register bit 7). If enabled the input signal is passed on to the IRQ15 output pin. Digital Audio : It used to provide a single amplitude (digital) audio waveform intended to be driven to the system's speaker.	59,122, 61,124	I	N/A

A_CADR<25:0> B3_CADR<25:0>	Socket A & B Card address : Address lines to the PCMCIA socket.	48,46,44,42,40,38, 36,34,32,41,43,35, 33,45,25,21,28,30, 47,49,50,53,55,57, 58,60, 110,108,106,104,1 02,100,98,96,94, 103,105,97, 95,107,89, 85,91,93, 109,112,113,115,1 18,120,121,123	TO	4ma
A_CD1#, A_CD2#, B_CD1#, B_CD2#	Card Detect : These signals are used to detect the presence of a card in the socket. The signals are connected to ground internally on the PC Card; thus they will be forced low whenever a card is placed in a host socket.	69,10, 132,73	I	N/A
A_PD<15:0> B_PD<15:0>	Socket A& B Data Bus : Data lines for the PCMCIA socket.	20,18,16,14,12,67, 65,63,17,15,13,11, 9,66,64,62 84,82,80,77,75,13 0,128, 126,81,78, 76,74,72, 129,127,125	B	4ma
A_OE#, B_OE#	Output Enable : This signal will be driven low for memory reads from the socket.	23,87	TO	4ma
A_WE#, B_WE#	Write Enable : This signal will be driven low for memory writes to the socket.	37,99	TO	4ma
A_IORD# B_IORD#	I/O Read : This signal will be driven low for I/O reads from the socket.	26,90	TO	4ma
A_IOWR# B_IOWR#	I/O Write : This signal will be driven low for writes to the socket.	29,92	TO	4ma
A_WP, B_WP (IOIS16#)	Write Protect : In memory mode, this is the status of the write protect status. Card is 16-bit Port : In I/O mode, this signal indicates that the I/O cycle being accessed is capable of 16-bit operation.	68,131	I	N/A
A_RDY/BSY# B_RDY/BSY# (IREQ#)	Ready/Busy : Driven low by memory card to indicate that the memory card is busy processing a previous command. This pin is set high when memory cards are ready to accept a new data transfer command. Interrupt Request : In I/O mode, this signal indicates an interrupt request.	39,101	I	N/A
A_INPACK# B_INPACK#	Input Acknowledge : This signal should be active during IORD cycles to which the card can respond.	56,119	I	N/A
A_REG# B_REG#	Attribute Memory Select : During PCMCIA memory cycles, this signal chooses between attribute and common memory. During I/O cycles, this signal is active. During DMA cycles, this signal is inactive.	8,71	TO	4ma

A_WAIT# B_WAIT#	Bus Cycle Wait : Signal driven by the PC Card to delay completion of the memory or I/O cycle which is in progress.	54,116	I	N/A
A_CE1#,A_CE2# B_CE1#,B_CE2#	Card Enable : Active low card enable signals driven by the chip. CE1# is used to enable even bytes, CE2# for odd bytes.	22,19 86,83	TO	4ma
A_RESET, B_RESET	Card Reset : Forces a hard reset to a PC Card.	51,114	TO	4ma
A_VPP_VCC B_VPP_VCC	This signal is used to enable the socket VCC supply onto the VPP pin. This pin is mutually exclusive with VPP_PGM.	2,205	O	12ma
A_VPP_PGM B_VPP_PGM	This signal is used to enable the programming voltage supply onto the VPP pin. This pin is mutually exclusive with VPP_VCC.	1,204	O	12ma
A_VCC_5# B_VCC_5#	This signal is used to enable a 5V supply onto the VDD socket.	5,207	O	12ma
A_VCC_3# B_VCC_3#	Not support, the chip is internally pull high.	4,206	O	12ma
A_DET_5 B_DET_5	Detect 5V : Reserve for detect 5V/3.3V.	6,7	I	N/A
A_SLOT_VCC B_SLOT_VCC	Reserve for mix voltage control to socket and chip.	24,52 88,117	I	N/A
Miscellaneous Control				
SPKCSEL#	Speaker Out/Chip Select : When power on reset, this pin is used as Chip Select. If the level is high when PWGOOD rises, this chip is configured to support socket 1 & 0, and the level is low the chip is used as socket 2&3. When PWGOOD is stable, this pin can be used to drive a speaker. It is the logical XOR of the speaker inputs from the sockets.	202	B	12ma
REFRESH	Refresh : This indicates a memory refresh cycle is taking place and will cause the chip to ignore memory accesses on the bus.	180	I	N/A
Power and Ground				
VDD	These pins are connected to 5V.	27,133,208	I	N/A
GND	These pins are connected to system ground.	31,70,79 111,140,192		

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	A_VPP_PGM	53	A_CADR4	105	B_CADR15	157	A23
2	A_VPP_VCC	54	A_WAIT#	106	B_CADR23	158	IO16
3	VPPVLD#	55	A_CADR3	107	B_CADR12	159	SBHE
4	A_VCC_3	56	A_INPACK#	108	B_CADR24	160	MS16#
5	A_VCC_5	57	A_CADR2	109	B_CADR7	161	A0
6	A_DET_5	58	A_CADR1	110	B_CADR25	162	A1
7	B_DET_5	59	A_BVD2	111	VSS	163	BCLK
8	A_REG#	60	A_CADR0	112	B_CADR6	164	A2
9	A_PD3	61	A_BVD1	113	B_CADR5	165	A3
10	A_CD1	62	A_PD0	114	B_RESET	166	BALE
11	A_PD4	63	A_PD8	115	B_CADR4	167	A4
12	A_PD11	64	A_PD1	116	B_WAIT#	168	A5
13	A_PD5	65	A_PD9	117	VDD	169	A6
14	A_PD12	66	A_PD2	118	B_CADR3	170	IRQ3
15	A_PD6	67	A_PD10	119	B_INPACK#	171	A7
16	A_PD13	68	A_WP	120	B_CADR2	172	IRQ4
17	A_PD7	69	A_CD2#	121	B_CADR1	173	A8
18	A_PD14	70	VSS	122	B_BVD2	174	IRQ5
19	A_CE1#	71	B_REG#	123	B_CADR0	175	A9
20	A_PD15	72	B_PD3	124	B_BVD1	176	A10
21	A_CADR10	73	B_CD1#	125	B_PD0	177	IRQ7
22	A_CE2#	74	B_PD4	126	B_PD8	178	A11
23	A_OE#	75	B_PD11	127	B_PD1	179	A12
24	VDD	76	B_PD5	128	B_PD9	180	REFRESH
25	A_CADR11	77	B_PD12	129	B_PD2	181	A13
26	A_IORD#	78	B_PD6	130	B_PD10	182	A14
27	VDD	79	VSS	131	B_WP	183	A15
28	A_CADR9	80	B_PD13	132	B_CD2#	184	A16
29	A_IOWR#	81	B_PD7	133	VDD	185	IOR#
30	A_CADR8	82	B_PD14	134	SD15	186	IOW#
31	VSS	83	B_CE1#	135	SD14	187	AEN
32	A_CADR17	84	B_PD15	136	SD13	188	IOCHRDY#
33	A_CADR13	85	B_CADR10	137	SD12	189	SD0
34	A_CADR18	86	B_CE2#	138	VDD	190	SD1
35	A_CADR14	87	B_OE#	139	SD11	191	NOWS#
36	A_CADR19	88	VDD	140	VSS	192	VSS
37	A_WE#	89	B_CADR11	141	SD10	193	SD2
38	A_CADR20	90	B_IORD#	142	SD9	194	SD3
39	A_RDYBSY	91	B_CADR9	143	SD8	195	VDD
40	A_CADR21	92	B_IOWR#	144	MEMW#	196	SD4
41	A_CADR16	93	B_CADR8	145	MEMR#	197	SD5
42	A_CADR22	94	B_CADR17	146	A17	198	IRQ9
43	A_CADR15	95	B_CADR13	147	A18	199	SD6
44	A_CADR23	96	B_CADR18	148	IRQ14	200	SD7
45	A_CADR12	97	B_CADR14	149	A19	201	PWRGD
46	A_CADR24	98	B_CADR19	150	IRQ15	202	SPKCSEL#
47	A_CADR7	99	B_WE#	151	A20	203	INTR#
48	A_CADR25	100	B_CADR20	152	IRQ12	204	B_VPP_PGM
49	A_CADR6	101	B_RDYBSY	153	A21	205	B_VPP_VCC
50	A_CADR5	102	B_CADR21	154	IRQ11	206	B_VCC_3
51	A_RESET	103	B_CADR16	155	A22	207	B_VCC_5
52	VDD	104	B_CADR22	156	IRQ10	208	VDD

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	^{o}C
Storate temperature	-55	125	^{o}C
Input voltage	-0.5	5.5	V
Output voltage	-0.5	5.5	V

Note :
Stress above these listed cause permanent damage to device. Functional operation of this evice should be restricted to the conditions described under operating conditions.

DC Characteristics

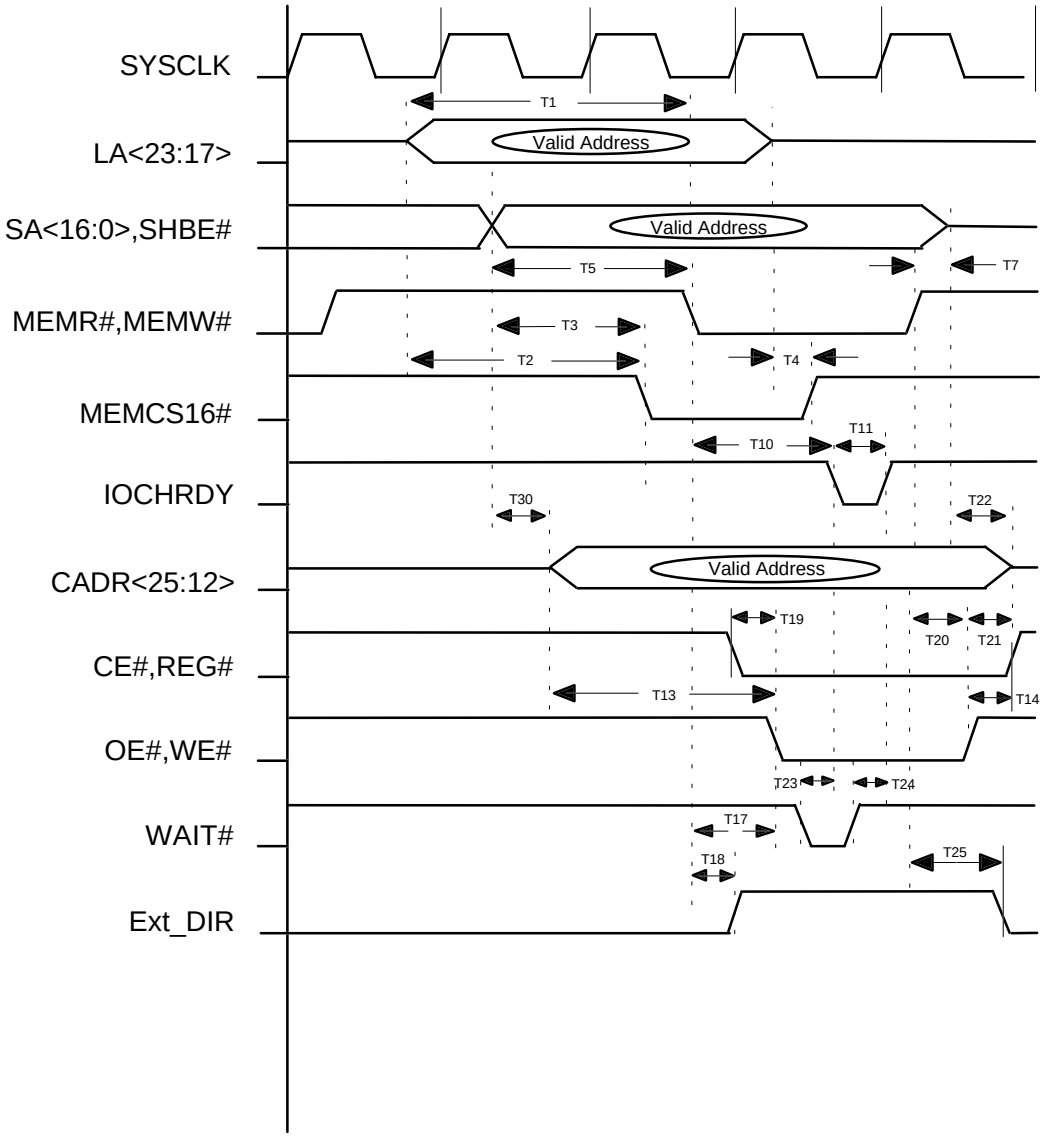
TA-0-70^{o}C, V_{DD}=5V=/-5%, GND=0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-.50	0.8	V	
V_{IH}	Imput high voltage	2.0	V_{DD}+0.5	V	
V_{OL}	Output low voltage	-	0.45	V	I_{OL}=4.0mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH}=-1.0mA
I_{IL}	Input leakage current	-	+/-10	uA	$0<V_{IN}<V_{DD}$
I_{OZ}	Tristate leakage current	-	+/-20	uA	$0.45<V_{OUT}<V_{DD}$
I_{CC}	Power supply current	-	80	mA	

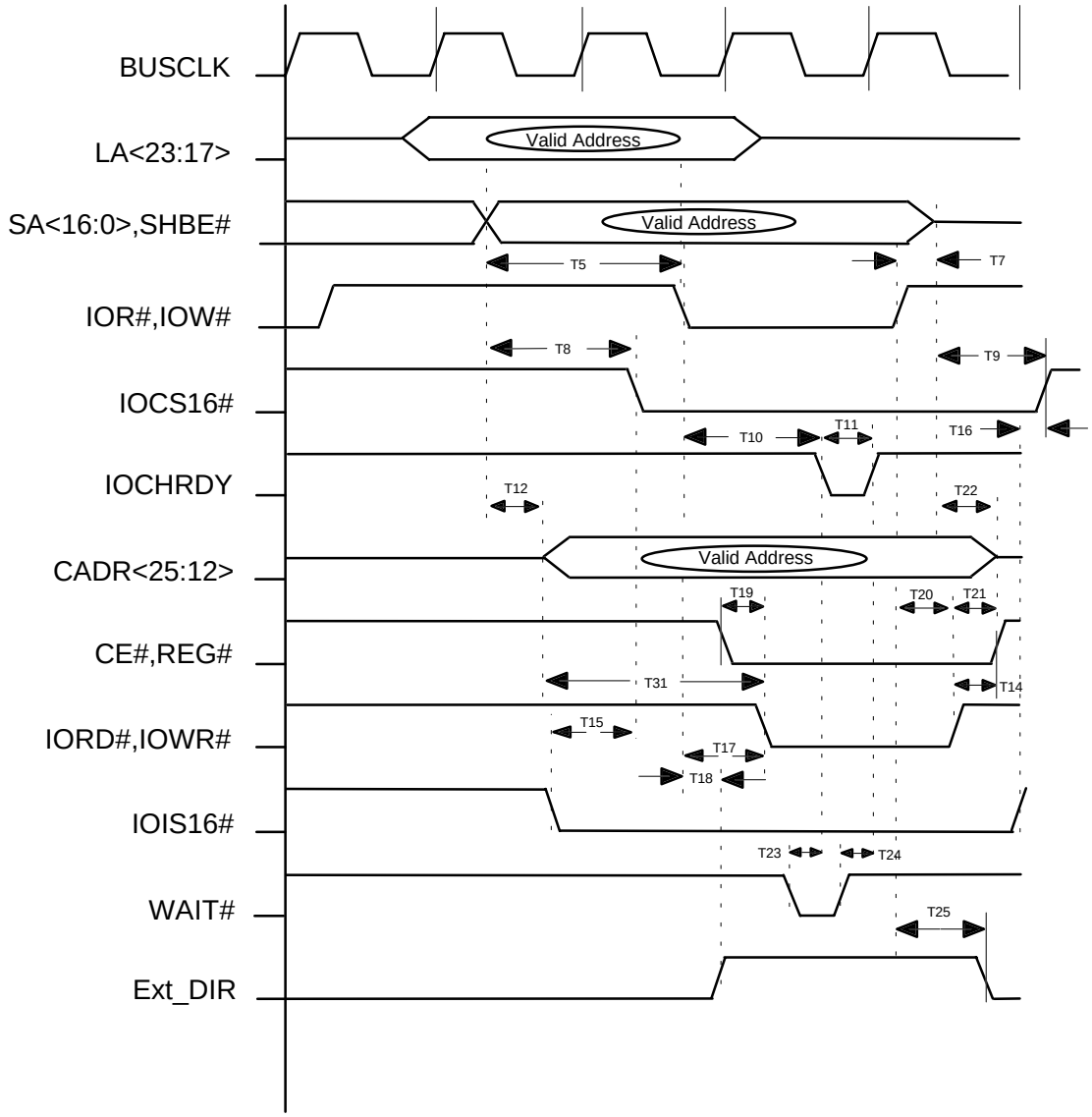
Parameter	Description	Min	Max
T1A	A<23:17> Setup to 16-Bit Memory Command	102	
T1B	A<23:17> Setup to 8-Bit Memory Command	162	
T2	MEMCS16# Valid from A<23:17>		58
T3	MEMCS16# Hold from A<16:00>		31
T4	MEMCS16# Hold from A<23:17>	0	
T5A	A<16:12> and SBHE# to 16-Bit Memory Command	18	
T5B	A<16:12> and SBHE# to 8-Bit Memory Command	84	
T5C	A<15:00> and SBHE# Setup to I/O Command	84	
T6	A<16:00> and SBHE# Hold from Command	25	
T7	IOCS16# Valid from A <15:00>		25
T8	IOCS16# Hold from A <15:00>	0	
T9	IOCHRDY Low from 16-Bit Command (Internal Wait State Generation)		20
T10	IOCHRDY Active Pulse Width (Memory Cycle) (Internal Wait State Generation)	123	363
T11	IOCHRDY Active Pulse Width (I/O Cycle) (Internal Wait State Generation)		63
T12A	A <15:12> to CA <25:12> Valid Delay, Memory Cycles		40
T12B	A <15:12> to CA <25:12> Valid Delay, I/O Cycles		26
T13A	CA <15:12> to Socket I/O CMD Setup	70	
T13B	CA <25:12> to Socket Memory CMD Setup	30	
T14A	Socket CMD to CE# Hold Time	20	
T14B	Socket CMD to REG# Hold Time	0	
T15	IOIS16# to IOCS16# Valid Delay		47
T16	IOCS16# Hold from IOIS16# Valid		12
T17	ISA CMD to SKT CMD Valid Delay for 8-Bit Memory, 8/16 I/O		22
T18	ISA Read CMD Falling to Data Output		21
T19	CE#, REG# Setup to Socket CMD Setup	5	
T20	ISA CMD Inactive to Socket CMD Inactive Valid Delay	0	20
T21	Socket CMD Inactive to CADR <25:12> Hold Time	20	
T22	CA <15:12> Hold from A <15:12> Memory	0	
T22	CA<15:12> Hold from A<15:12> I/O	0	

T23	WAIT# Active to IOCHRDY Inactive		16
T24	WAIT# Inactive to IOCHRDY Active		14
T25	EXT_DIR Hold from ISA Read Inactive	0	
T26	AEN Valid to ISA CMD Active Setup	40	
T27	AEN Hold from ISA Command Inactive	5	
T28	RI_to RI_OUT Delay		27
T29	SPKR_ to SPKR_OUT Delay		18
T30	Card Status Change to IRQ# Valid		7 BUSCLK
T31	PCMCIA IREQ# to IRQx Delay		24

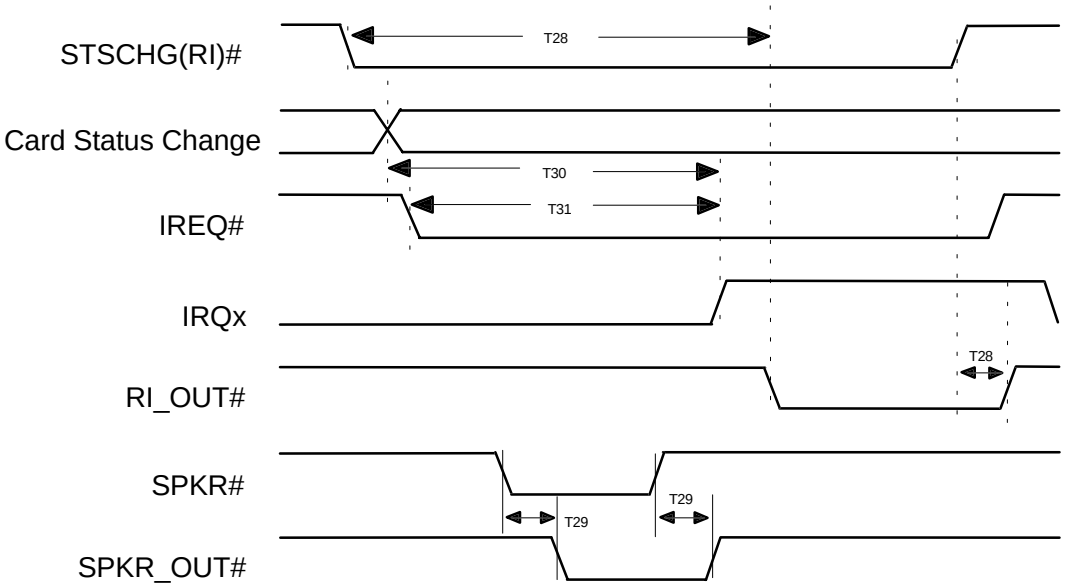
Memory: Standard/Extended



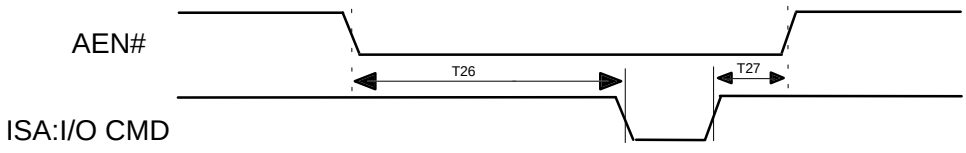
IO: Standard / Extended



Interrupt, Ring Indicate, Speaker Timings



AEN Setup and Hold



208-Pin Plastic Flat Package