Winbond Electronics Corp.

PCMCIA ETHERNET NETWORK TWISTED PAIR INTERFACE CONTROLLER

GENERAL DESCRIPTION

The W89C926 PENTIC+ is a CMOS device designed for easy implementation of PCMCIA R2.1 compatible CSMA/CD local area networks. The W89C926 combines a W89C902 Serial LAN Coprocessor for Twisted-pair (SLCT) with a PCMCIA Bus Interface (PBI), thus integrating into a single chip all the registers and logic necessary to connect the SLCT to buffer SRAMs, flash memories (or an EEPROM), and the PCMCIA system bus.

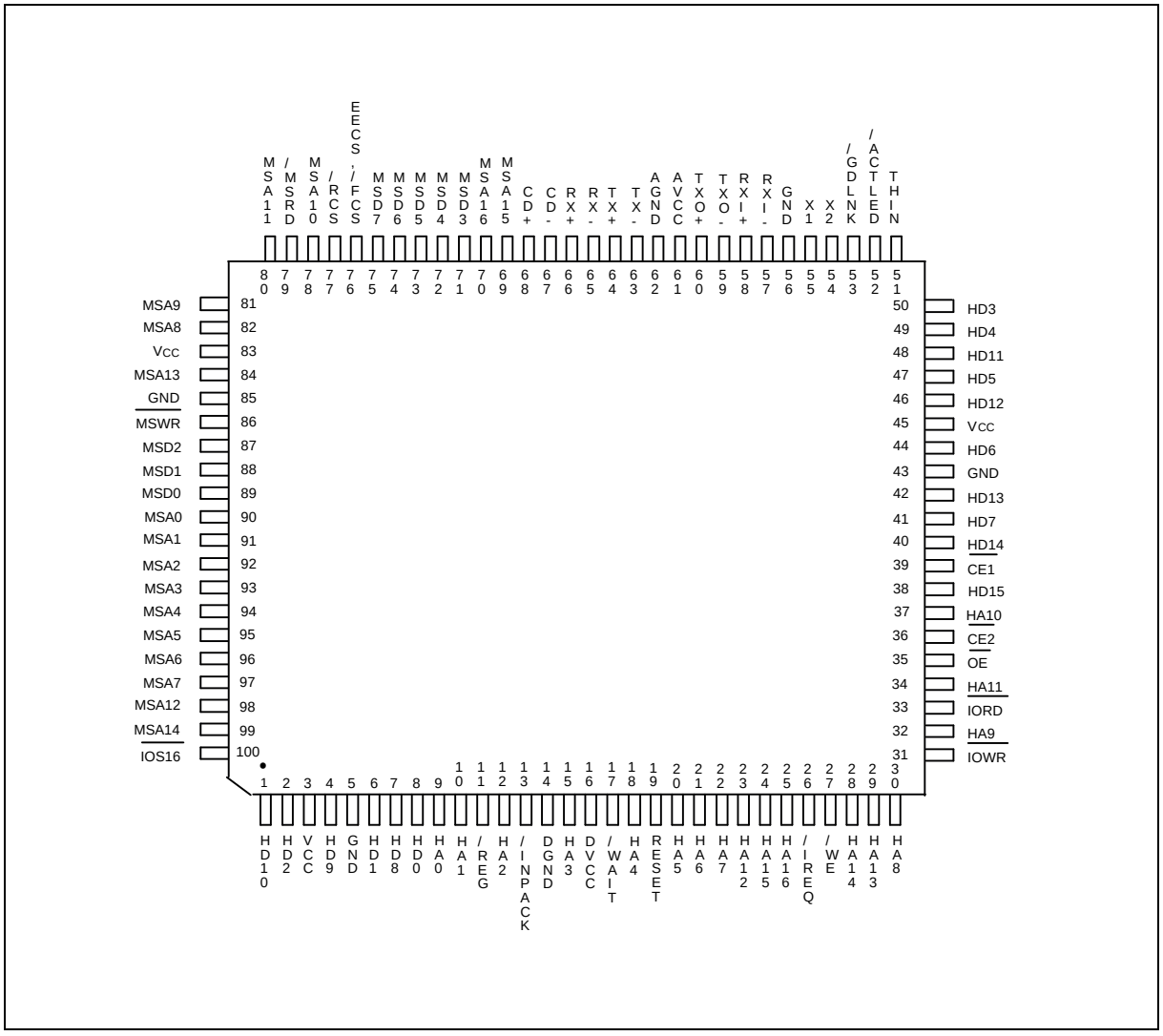
The PCMCIA Bus Interface (PBI) is designed to provide a switchless setting architecture that allows the card setting to be configured by software. It implements a full set of PCMCIA registers for PCMCIA R2.1 compatibility and a set of configuration registers for switchless card setting. The card can be configured quickly and easily by modifying the contents of the configuration registers. The PENTIC+ can run with shared memory mode and NE2000™ I/O mode drivers on a 16-bit bus interface. No extra effort is needed to ensure software compatibility.

The PENTIC+ provides a flexible flash memory (up to 128 KB)/EEPROM (up to 512 bytes) architecture for PCMCIA nonvolatile storage and an ID/Configuration auto-load architecture for power-on initialization. Vendors can store the Ethernet® ID, configuration, and CIS in the flash memory or EEPROM. The PENTIC+ will auto-load necessary information when power is switched on.

FEATURES

- Runs with NE2000 ™ or shared memory drivers
- Supports up to 128 KB flash memory (8K/112K for attribute/common memory) or 512 bytes EEPROM (for attribute memory only) for nonvolatile memory
- Uses one 16 KB SRAM or one 32 KB SRAM (if EEPROM is used) for 16 KB Ethernet ring buffer
- Auto-load algorithm provided for power-on initialization
- Supports necessary PCMCIA registers
- Configuration registers allow switchless card setting
- UTP/BNC auto media-switching function provided
- Drives necessary LEDs for network status display
- Single 5V power supply with low power consumption
- 100-pin thin package (TQFP) fits into PCMCIA Type II profile

PIN CONFIGURATION



PIN DESCRIPTION

NAME	NUMBER	TYPE	DESCRIPTION
PCMCIA Bus Interface			
HA0-2 HA3, 4 HA5-7 HA8-10 HA11-13 HA14-16	9, 10, 12 15, 18 20-22 30, 32, 37 34, 23,29 28, 24, 25	I/TTL	Host Address Bus: Host address lines used to decode access to the card's memory and I/O spaces.
HD0-2 HD3-5 HD6-8 HD9-11 HD12-15	8, 6, 2 50, 49, 47 44, 41, 7 4, 1, 48 46, 42, 40, 38	IO/3SH	Host Data Bus: Bidirectional host data bus.
$\overline{\text{IREQ}}$	26	O/TTL	Interrupt Request: $\overline{\text{IREQ}}$ is asserted by the PENTIC+ to request host service. During auto-loading, which is caused by a H/W reset, $\overline{\text{IREQ}}$ will assert low until auto-loading is complete. This signaling is used as Rdy/-Bsy of Memory Only Interface during initialization, according to PCMCIA R2.1.
$\overline{\text{IORD}}$	33	I/TTL	I/O Read: $\overline{\text{IORD}}$ is asserted by the system to read data from the card's I/O space. It has an internal 100K ohm pull-high resistor.
$\overline{\text{IOWR}}$	31	I/TTL	I/O Write: $\overline{\text{IOWR}}$ is asserted by the system to write data to the card's I/O space. It has an internal 100K ohm pull-high resistor.
$\overline{\text{WE}}$	27	I/TTL	Write Enable: The $\overline{\text{WE}}$ input is asserted by the system to strobe memory write data into the card memory. It has an internal 100K ohm pull-high resistor.

Pin Description, continued

NAME	NUMBER	TYPE	DESCRIPTION
$\overline{OE}$	35	I/TTL	Output Enable: The $\overline{OE}$ line is asserted by the system to obtain memory read data from the card memory. It has an internal 100K ohm pull-high resistor.
$\overline{CE1,2}$	39, 36	I/TTL	Card Enable: $\overline{CE1,2}$ are asserted by the system for data bus width control as shown below. These pins have an internal 100K ohm pull-high resistor.

$\overline{CE2}$	$\overline{CE}$	HD15-HD8	HD7-HD0
0	0	Valid	Valid
0	1	Valid	High-Z
1	0	High-Z	Valid
1	1	High-Z	High-Z

$\overline{REG}$	11	I/TTL	Register & I/O selection: $\overline{REG}$ is asserted by the system to access attribute memory or I/O space. It remains high inactive for common memory accesses. It has an internal 100K ohm pull-high resistor.
$\overline{IOIS16}$	100	O/TTL	16-bit I/O access: Asserted by the PENTIC+ to inform the system that current operation is a 16-bit I/O access.
$\overline{INPACK}$	13	O/TTL	Input Acknowledge: Asserted by the PENTIC+ when it has been selected and can respond to an I/O read cycle.
$\overline{WAIT}$	17	O/TTL	Wait State: Asserted by the PENTIC+ to insert wait states into current memory or I/O access cycles.
RESET	19	I/TTL	Card Reset: A RESET pulse will initiate the PENTIC+'s initialization procedure, including auto-ID/configuration loading, register initialization, and state machine initialization. The pulse width should be at least 500 nS to be recognized as a valid reset. This pin has an internal 100K ohm pull-up resistor.

Pin Description, continued

NAME	NUMBER	TYPE	DESCRIPTION
Memory Support Interface			
MSA0-7 MSA8-10 MSA11-13 MSA14-16	90-97 82, 81, 78 80, 98, 84 99, 69, 70	O/TTL	Memory Support Address: Latched address used to decode accesses to the on-board memory.
MSD0-2 MSD3-7	89-87 71-75	IO/3SH I/O/3SH	Memory Support Data Bus: Bidirectional on-board memory data bus. EEPROM Interface: During the EEPROM auto-load or read/write sequence, MSD0 is used as a serial data input/output from/to EEPROM, MSD1 outputs EEPROM commands to EEPROM, and MSD2 sends a clock with a period of 1.2 microseconds. This function is available only when EECS/$\overline{\text{FCS}}$ is low during H/W reset.
$\overline{\text{RCS}}$	77	O/TTL	SRAM Chip Select: $\overline{\text{RCS}}$ is asserted by the PENTIC+ for SRAM chip enable during buffer memory access.
EECS/$\overline{\text{FCS}}$	76	O/3SH I/3SH	Nonvolatile Memory Chip Select: EECS/$\overline{\text{FCS}}$ is asserted by the PENTIC+ for chip enable during nonvolatile memory access. It is active low for flash memory enable and active high for EEPROM chip enable. Nonvolatile Memory Detection: During H/W reset, the PENTIC+ will determine the existing nonvolatile memory type by sampling the voltage level on this pin. If this pin is externally pulled high with a 470K ohm resistor, the PENTIC+ will determine that the memory is a flash memory; if the pin is pulled low with a 470K ohm resistor, it will determine that the memory is an EEPROM.
$\overline{\text{MSRD}}$	79	O/TTL	Memory Support Read: $\overline{\text{MSRD}}$ is asserted by the PENTIC+ to strobe read data from the on-board memory. Both SRAM and flash memory use $\overline{\text{MSRD}}$ as the read command strobe.

Pin Description, continued

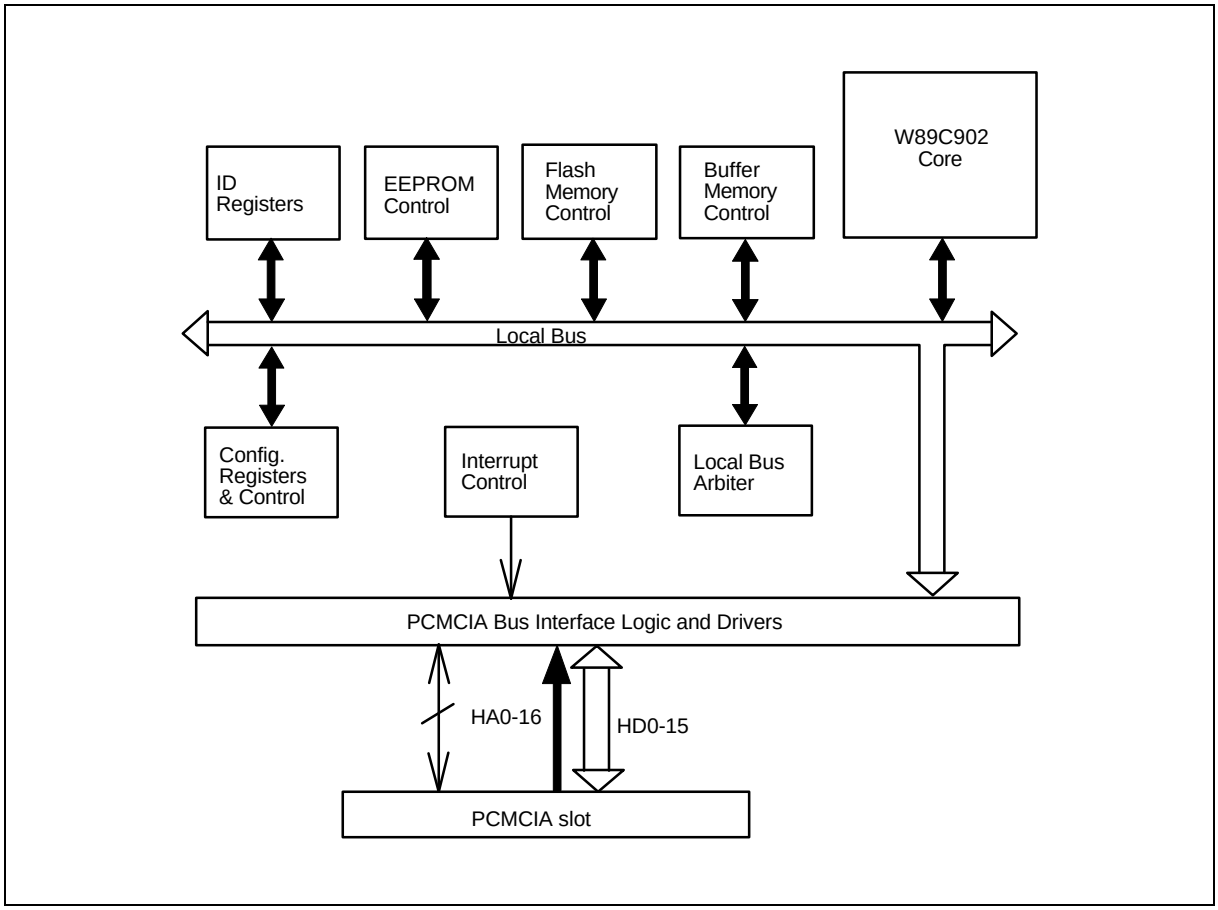
NAME	NUMBER	TYPE	DESCRIPTION
$\overline{\text{MSWR}}$	86	O/TTL	Memory Support Write: $\overline{\text{MSWR}}$ is asserted by the PENTIC+ to strobe write data into the on-board memory. Both SRAM and flash memory use $\overline{\text{MSWR}}$ as the write command strobe.
Network Interface			
TXO+, -	60, 59	O/DIF	Twisted Pair Transmit Outputs: UTP differential output pair. A 1.21 KΩ precision resistor should be shunted across these pins for signal pre-equalization.
RXI+, -	58, 57	I/DIF	Twisted Pair Receive Inputs: These inputs are fed into a differential amplifier which passes valid data to the LCE core. A 100Ω precision resistor should be shunted across these pins for impedance matching.
TX+, -	64, 63	O/DIF	AUI Transmit Outputs: Differential transmit outputs. These pins should be connected to 270 ohm external pull-down resistors.
RX+, -	66, 65	I/DIF	AUI Receive Inputs: Differential receive input pair from AUI interface.
CD+, -	68, 67	I/DIF	AUI Collision Inputs: Differential collision input pair from AUI interface.
X1	55	I/XTAL	Crystal Input: Master 20 MHz clock input.
X2	54	O/XTAL	Crystal Feedback Output: This pin should be connected to the crystal when a crystal is used and should be left unconnected when an oscillator is used.
THIN	51	O/TTL	Thin Cable Select: This pin is high when the PENTIC+ is configured for thin cable media. It can be used as a switch to DC-DC converter for network media selection.
$\overline{\text{ACTLED}}$	52	O/TTL	Activity: This output asserts low for approximately 50 mS whenever the PENTIC+ transmits or receives data without collisions. This output can also be controlled by the power-down state machine; refer to the descriptions of the COR and CFA registers for more details.

Pin Description, continued

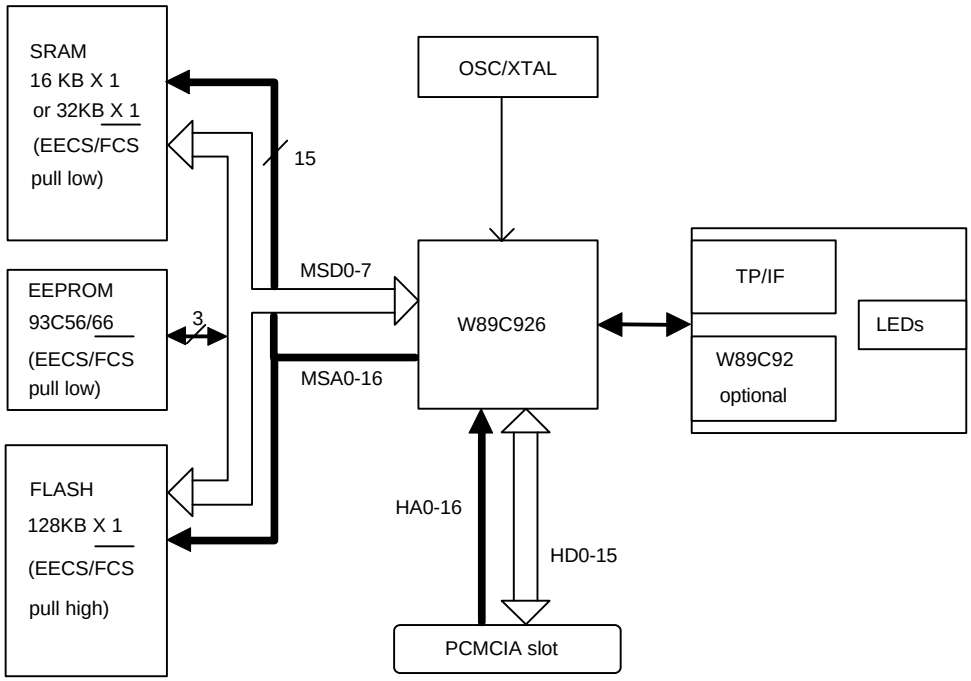
NAME	NUMBER	TYPE	DESCRIPTION
$\overline{\text{GDLNK}}$	53	O/TTL	GoodLink: This output asserts low if the PENTIC+ is in TPI mode, link checking is enabled, and the link integrity is good or if link checking is disabled; otherwise, is not asserted. This output can also be controlled by power down state machine; refer to the description of the COR and CFA registers for more details.
Power Pins			
AVCC	61		Analog Power Supply Pins: These pins supply +5V to the PENTIC+'s analog circuitry for the network interface. Analog layout rules and decoupling methods must be applied between this pin and AGND.
AGND	62		Analog Ground Pins: These pins are the ground to the analog circuitry.
VCC	3, 16, 45, 83		Digital Power Supply Pins: These pins supply +5V to the PENTIC+'s digital circuitry.
GND	5, 14, 43, 56, 85		Digital Ground Pins: These pins are the ground to the digital circuitry.

Note: I: input pin; O: output pin; IO: bidirectional input/output pin; TTL: TTL level buffer stage; ODH: open drain buffer stage; MOS: MOS level buffer stage; 3SH: Tri-state buffer stage; DIF: differential buffer stage, XTAL: crystal.

BLOCK DIAGRAM



SYSTEM DIAGRAM



Two combinations may be used for the hardware structure:

Combination 1: EECS/FCS pull high/128 KB X 1 flash memory/16 KB X 1 SRAM

Combination 2: EECS/FCS pull low/256 or 512B EEPROM/32 KB X 1 SRAM

FUNCTIONAL DESCRIPTION

ADDRESS MAPPING

EEPROM MAPPING

EEPROM ADDRESS	HIGH BYTE	LOW BYTE
00H	-	Word Count
01H	CFB	CFA
02H	ID-1	ID-0
03H	ID-3	ID-2
04H	ID-5	ID-4
05H	Check Sum	Board Type (05H)
06H-08H	-	-
09H	57H	57H
0AH-nH	CIS	CIS
(n+1) H-FFH	-	-

Notes:

1. The fifth (05H) word is used for shared memory mode and the ninth (09H) word is used for NE2000 mode.
2. Word Count = nH (n should be set as a non zero value, a zero value will cause an unpredicted error).

ATTRIBUTE MEMORY MAPPING

EECS/$\overline{\text{FCS}}$ Pull High (Flash Memory)

ATTRIBUTE MEMORY OFFSET (HA0-16)	TYPE	CONTENTS
00000H 00F9EH	Flash	CIS
00FA0H	Flash	ID-0
00FA2H	Flash	ID-1
00FA4H	Flash	ID-2
00FA6H	Flash	ID-3
00FA8H	Flash	ID-4
00FAAH	Flash	ID-5
00FACH	Flash	Board Type (05H)
00FAEH	Flash	Check Sum
00FB0H	Flash	-
00FB2H	Flash	-
00FB4H	Flash	-
00FB6H	Flash	-
00FB8H	Flash	-
00FBAH	Flash	-
00FBCH	Flash	57H
00FBEH	Flash	57H
00FC0H	Flash	CFA
00FC2H	Flash	CFB
-	-	-
00FD0H	Register	COR
00FD2H	Register	CCSR
00FD4H	Register	-
00FD6H	Register	SCR
-	Register	Reserved (see note)
00FF0H	Register	CFA
00FF2H	Register	CFB
00FF4H	Register	SR
00FF6H 00FFEH	Register	Reserved
01000H 03FFEH	Flash	CIS

EECS/$\overline{FCS}$ Pull Low (EEPROM)

ATTRIBUTE MEMORY OFFSET (HA0-16)	TYPE	CONTENTS
00000H 003D6H	Memory (SRAM)	CIS
-	Unsued	-
00FD0H	Register	COR
00FD2H	Register	CCSR
00FD4H	Register	-
00FD6H	Register	SCR
-	Register	Reserved (see note)
00FF0H	Register	CFA
00FF2H	Register	CFB
00FF4H	Register	SR
00FF6H 00FFEH	Register	Reserved
01000H 03FFEH	Unused	-

Notes:

1.The reserved register space in the attribute space is left for future extension. Users should not place their application in this area.

2. When EECS/$\overline{FCS}$ is pulled high, address 00FA0H to 00FFEH is used for Ethernet ID, configuration, and registers. Vendors should not put CIS in this region.

3. When EECS/$\overline{FCS}$ is pulled low, Address 00000H to 003D6H is read-only. The PENTIC+ will ignore write accesses to this area.

NE2000 Mode Mapping

I/O Mapping

SYSTEM I/O OFFSET (HA0-4)	NAME	OPERATION
00H 0FH	LCE Core Registers	Register Read/Write
10H 17H	Remote DMA Port	Remote DMA Read/Write
18H 1FH	Reset Port	Software Reset

Notes:

1. The PENTIC+ decodes only HA0-4 for I/O access, so the IOBase address is left for the host adapter and the socket service to determine.

2. To issue a S/W reset, simply issue an I/O read to the Reset Port. The PENTIC+ will assert a 600 nS internal reset pulse to reset the core state machine. If the host tries to access the PENTIC+, $\overline{WAIT}$ will be asserted low until the reset is completed.

Buffer Memory Mapping

NIC CORE MEMORY MAP	NE2000 COMPATIBLE
0000H 001FH	ID Registers
0020H 00FFH	Aliased
0100H 3FFFH	ID Registers
4000H 7FFFH	Buffer SRAM (16K × 8)
8000H BFFFH	Aliased ID Registers
C000H FFFFH	Aliased Buffer SRAM

Nonvolatile Memory Mapping

F/$\overline{EE}$ = 1 (flash memory used)

SYSTEM OFFSET (HA0-16)	MEMORY TYPE	NAME
00000H 03FFFH	Attribute/ Flash	CIS/ID/PCMCIA Register (8K × 8)
04000H 1FFFFH	Common/ Flash	(112K × 8)

F/$\overline{EE}$ = 0 (EEPROM used)

SYSTEM OFFSET (HA0-16)	MEMORY TYPE	NAME
00000H 003D6H	Attribute/ (Note)	CIS (492 × 8)

Notes:
1. This attribute memory is an image from EEPROM. It is actually resident in upper half of the SRAM after power-on auto-loading.
2. Refer to "Attribute Memory Mapping" for detailed locations.
3. The PENTIC+ decodes HA0-16 for memory access. The (common or attribute) MEMBase addresses are left for the host adapter and the socket service to determine.

Shared Memory Mode Mapping

I/O Mapping

SYSTEM I/O OFFSET (HA0-4)	NAME	OPERATION
00H	MMA	I/O Write
01H	Word/-Byte	I/O Read
05H	MMB	I/O Write
08H 0FH	ID Registers	I/O Read
10H 1FH	LCE Core Registers	Register Read/Write

Notes:

1. The PENTIC+ decodes only HA0-4 for I/O access, so the IOBase address is left for the host adapter and the socket service to determine.
2. MMA and MMB are used for shared memory mapping control. Since the PENTIC+ decodes only MSA = 0000H to 03FFFH for shared memory that is, the shared memory base address for the PENTIC+ is 00000H, MMB and bit 0 to 5 of MMA should be set to 0.
3. Since the PENTIC+ supports 16-bit mode only, the Word/-Byte will be read as 01H.

Buffer Memory Mapping

SYSTEM OFFSET (HA0-16)	MEMORY TYPE	SHARED MEMORY MODE
00000H 03FFFH	Common/SRAM	Buffer SRAM (16K × 8)
04000H 07FFFH	Common/(Note)	Unused

Notes:

1. This region is occupied by flash memory.
2. The PENTIC+ decodes HA0-16 for memory access. The (common or attribute) MEMBase addresses are left for the host adapter and the socket service to determine.

Nonvolatile Memory Mapping

F/$\overline{EE}$ = 1 (flash memory used)

SYSTEM OFFSET (HA0-16)	MEMORY TYPE	NAME
00000H 03FFFH	Attribute/ Flash	CIS/ID/PCMCIA Register (8K × 8)
04000H 1FFFFH	Common/ Flash	 (112K × 8)

F/$\overline{EE}$ = 0 (EEPROM used)

SYSTEM OFFSET (HA0-16)	MEMORY TYPE	NAME
00000H 003D6H	Attribute/ (Note)	CIS (492x 8)

Notes:

1. This attribute memory is an image from EEPROM. It is physically resident in upper half of the SRAM after power-on auto-loading.
2. Refer to "Attribute Memory Mapping" for detailed locations.
3. The PENTIC+ decodes HA0-16 for memory access. The (common or attribute) MEMBase addresses are left for the host adapter and the socket service to determine.

REGISTER FILE

The W89C926 PENTIC+ has four register sets: the core register set, the PCMCIA configuration register set, the LAN configuration register set, and the special control register set. The core register set is the same as that in the W89C90 and will not be discussed here. The other three register sets are described below.

PCMCIA Configuration Register Set

The PENTIC+ provides three PCMCIA configuration registers needed to ensure compatibility with various operating systems.

COR (Configuration Option Register)

Access Address: AMBase + 00FD0H

Access Type: Attribute Memory Read/Write

BIT	SYMBOL	DESCRIPTION
0-5	IDX0-5	Configuration Index These six bits are used to indicate entry of the card configuration table located in the CIS (Card Information Structure; refer to PCMCIA R2.1). These bits are 0 at power-on.
6	-	Reserved, must be 1 (level mode interrupt) when read.
7	SRESET	S/W Reset A software reset is issued when a 1 is written to this bit. This is the same as a H/W reset except that this bit and the necessary information (CFA, CFB, CIS, and Ethernet ID) are not cleared, and the auto-load procedure is not performed. Returning a 0 to this bit will leave the PENTIC+ in a post-reset state the same as that following a hardware reset. The value of this bit at power-on is 0.

CCSR (Card Configuration and Status Register)

Access Address: AMBase + 00FD2H

Access Type: Attribute Memory Read/Write

BIT	SYMBOL	DESCRIPTION
0	-	Reserved, must be 0.
1	Intr	Interrupt Status This bit indicates the internal status of an interrupt request. It remains high until the condition that caused the interrupt request has been serviced. This bit is 0 at power-on.
2-7	-	Reserved, must be 0s.

SCR (Socket and Copy Register)

The SCR is used to enable the PENTIC+ to distinguish between similar cards installed in the same system.

Access Address: AMBase + 00FD6H

Access Type: Attribute Memory Read/Write

BIT	SYMBOL	DESCRIPTION
0-3	SocNum	Socket Number Set these bits to indicate to the PENTIC+ that it is located in the n'th socket. The first socket is numbered 0. This permits any cards designed to do so to share a common set of IO ports while remaining uniquely identifiable. These bits are 0 at power-on.
4-6	CopNum	Copy Number Set these bits to indicate to the PENTIC+ that it is the n'th copy of another card installed in the system that is configured identically. The first identical card should be assigned a value of 0 as its copy number. This permits any cards designed to do so to share a common set of I/O ports while remaining uniquely identifiable and consecutively ordered. These bits are 0s at power-on.
7	-	Reserved, must be 0.

LAN Configuration Register Set

These two registers are used for LAN configuration control.

CFA (Configuration Register A)

This register is used to select the PENTIC+'s operating mode and LED control.

Access Address: AMBase + 00FF0H

Access Type: Attribute Memory Read/Write

BIT	SYMBOL	DESCRIPTION
0	M/-IO	Share Memory/IO Mode Select The PENTIC+ will operate in shared memory mode if this bit is high; otherwise, it will be in I/O mode.
1-5	-	Reserved, must be 0s.
6	F/$\overline{EE}$	Flash or EEPROM Select. This bit directly reflects the sampled value on pin EECS/$\overline{FCS}$ during a H/W reset. This bit will be high or low if EECS/$\overline{FCS}$ is pulled high or low. This bit is read-only.
7	LED	LED Disable. Setting this bit high disables the LED indicators in order to save power.

CFB (Configuration Register B)

Access Address: AMBase + 00FF2H

Access Type: Attribute Memory Read/Write

BIT	SYMBOL	DESCRIPTION
0-1	PHY01	Physical Media Select These two bits determine to which type of medium the PENTIC+ is attached. The THIN pin will output low in 10BASE5 mode and high in 10BASE2 mode, according to PHY0,1. This can be used to control the DC-DC converter for electrical isolation.

PHY1	PHY0	Attached Medium Type
0	0	TPI (10BASE-T Compatible Squelch Level)
0	1	Thin Ethernet (10BASE2)
1	0	Thick Ethernet (10BASE5)
1	1	TPI (Reduced Squelch Level)

The PENTIC+ also provides a UTP/BNC auto media-switching function. The physical interface will jump from UTP to BNC when the PENTIC+ is configured at UTP, the link checking is enabled, and the UTP path is broken. It will jump back immediately if the UTP path has been reconnected. When the physical interface is not configured at TPI or the link checking is disabled, the auto media-switching function will be disabled.

CFB (Configuration Register B), continued

BIT	SYMBOL	DESCRIPTION
2	LNKEN	Link Enable Writing a "1" to this bit will disable the link pulse generation, auto media-switching function, and link integrity check function. Writing a "0" to this bit will enable these functions.
3	LNKSTS	Link Status This bit indicates the present link status. It is high if the PENTIC+ is in TPI mode, the link checking is enabled, and the link integrity is good or if the link checking is disabled; otherwise, it is low.
4	IO16CON	IOIS16 Timing Control. If this bit is set high, the IOIS16 signal will decode $\overline{CE1,2}$; otherwise, IOIS16 is decoded according to HA and REG (default).
5	FWEN	Flash Write Enable. The default setting for the flash memory is write-protected. If FWEN = 1, the PENTIC+ allows the flash to be written to. The write command and chip select signal is prohibited if FWEN = 0.
6	SRAMSEL	SRAM Speed Select. If SRAMSEL = 1, the SRAM-15 is selected. Otherwise, SRAM-70 is used. The default is SRAM-70.
7	-	Reserved.

Special Control Register Set

These registers are used for special checking or EEPROM access control.

Signature Register (SR)

A signature register is used for identification so that the software driver can easily distinguish between different chips. The content can be read out in toggled order as follows:

Access Address: AMBase + 00FF4H

Access Type: Attribute Memory Read

	MSB LSB	
(2N)th time:	10001000	where N = 1, 2, ... (after H/W reset)
(2N-1)th time:	00000000	

EEPROM Access Register (EEAR)

This register is located on page 3 and is used for EEPROM read/write access control. It is inhibited when EECS/$\overline{FCS}$ is pulled high.

Access Address: IOBase + 02H

Access Type: I/O Read/Write

BIT	SYMBOL	DESCRIPTION
0-5	-	Reserved. Must be 0s.
6	EW/$\overline{ER}$	EEPROM Write/Read Select. This bit selects the EEPROM read/write sequence. If EW/$\overline{ER}$ = 1, the write sequence is selected. If EW/$\overline{ER}$ = 0, the read sequence is selected.
7	EOS	EEPROM Operation Select. This bit enables the EEPROM read/write sequence. If EOS = 1, the EEPROM read/write sequence will be started. EOS is reset if the read/write sequence is finished or aborted.

EEPROM Address/Data Register (ADR)

This register is located on page 3 and is used for EEPROM address or data transfer during EEPROM access.

Access Address: IOBase + 04H

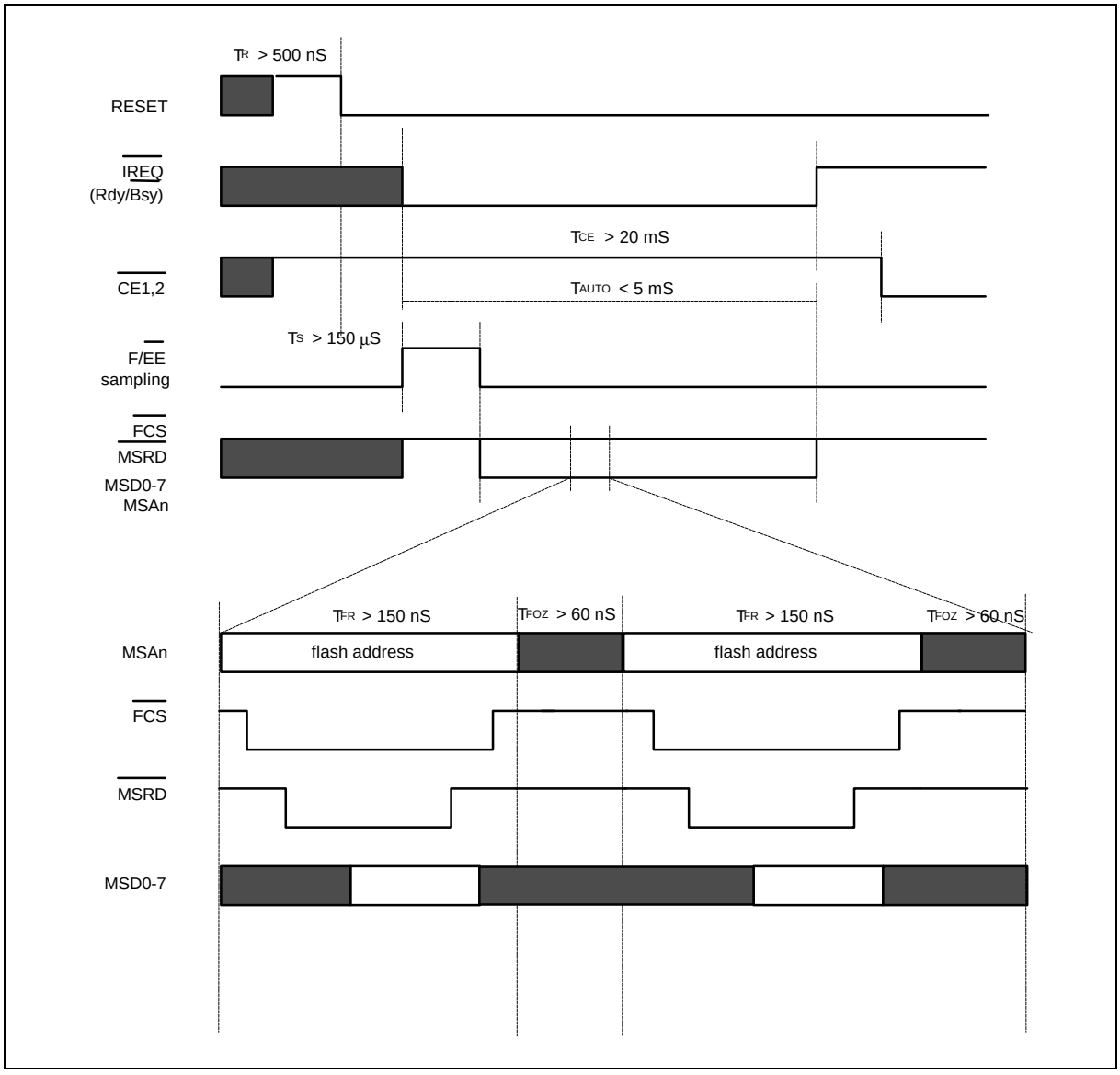
Access Type: I/O Read/Write

POWER-ON INITIALIZATION AND AUTO-LOADING PROCESS

When powered on, the system should reset the card first, as required by the PCMCIA specifications. The reset signal will trigger a number of internal operations: First, the PENTIC+ monitors the EECS/$\overline{FCS}$ pin to determined where the configurations are stored. If this pin is pulled high, the configurations are stored in the flash memory; if it is pulled low, they are stored in an EEPROM. Then, within 10ms after the reset pulse is negated, the PENTIC+ will automatically load the configurations, ID, and CIS data into the LAN configuration registers and the upper half of SRAM (if an EEPROM is used). During this auto-load procedure the PENTIC+ will assert $\overline{IREQ}$ low for Rdy/Bsy signaling, since the socket is configured at the memory-only interface during initialization. Note that this auto-load operation occurs only after a hardware reset pulse. A software reset (including setting COR.SRESET = 1) will not invoke this operation.

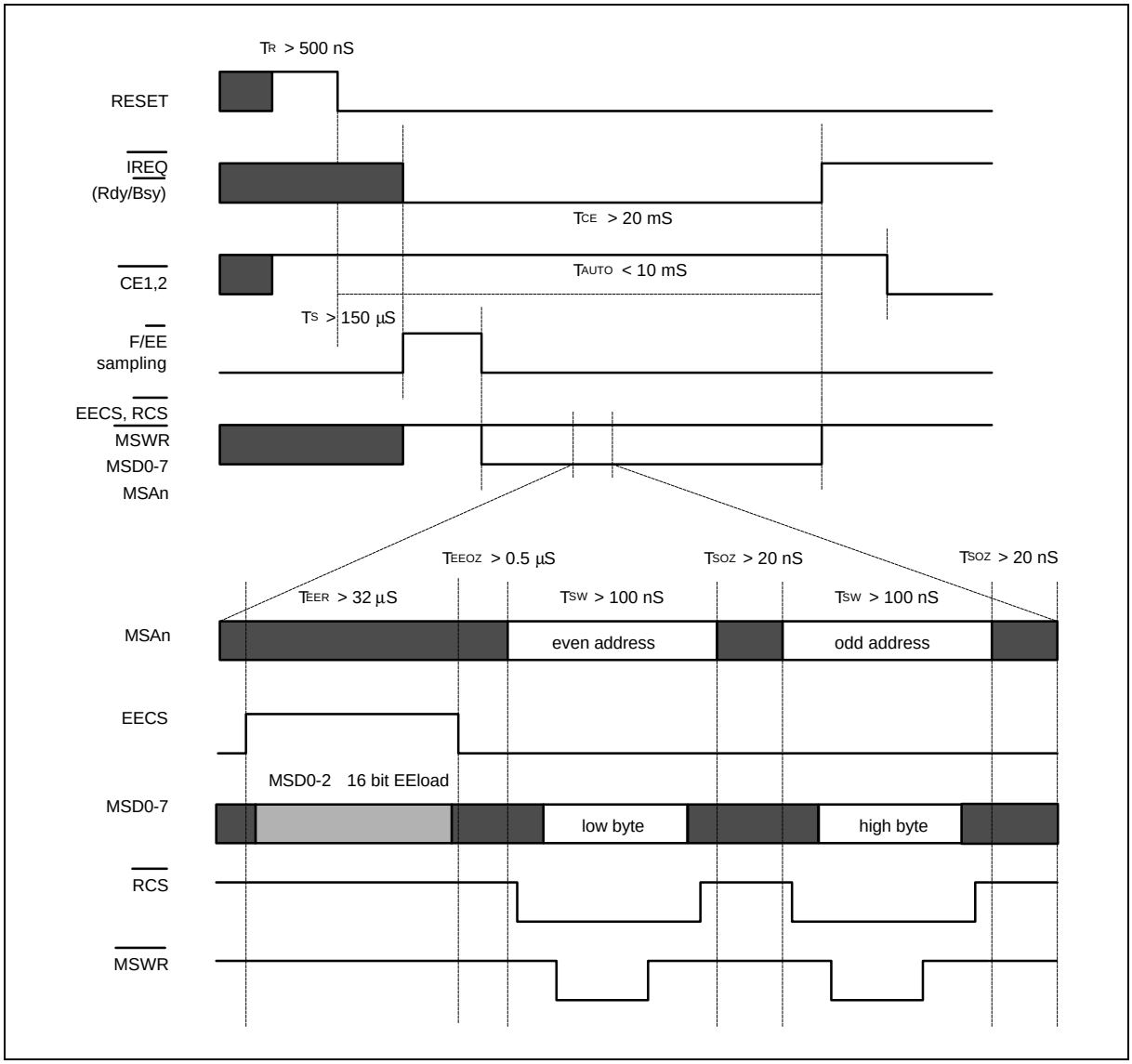
EECS/$\overline{FCS}$ Pulled High

If EECS/$\overline{FCS}$ is pulled high, this indicates that the configurations are stored in a flash memory. Accordingly, after a power-on reset the PENTIC+ will automatically load the LAN configuration registers from flash memory. The Ethernet IDs stored in the flash memory will be mapped into ID registers automatically when they are read.



EECS/$\overline{\text{FCS}}$ Pulled Low

If EECS/$\overline{\text{FCS}}$ is pulled low, this indicates that the configurations, Ethernet ID, and CIS are stored in an EEPROM. In this case, after a power-on reset the PENTIC+ will load the configurations into the LAN configuration registers and the Ethernet IDs and CIS into the higher half of SRAM memory (with auto-mapping to ID registers and attribute memory space, respectively). Since the EEPROM used is a 93C66, a serial EEPROM storage device, the access time is quite long and the system has to wait for the loading sequence (refer to PCMCIA R2.1). Loading a word of EEPROM typically takes 34 µS. The exact time for EEPROM loading depends on the length of CIS but must not exceed 10 mS.



EEPROM Contents Load Back

When an EEPROM is used to store CIS, the PENTIC+ allows the contents of the EEPROM to be modified by means of the following sequence:

```
write (EEAR, EOS = 1 EW/ER = 1)
write (ADR, address);
write (ADR, word_data);
wait (  );
repeat (
        read(EEAR, EOS);
        ) until (EOS = 0);
/* The entire sequence should be consecutive or the process will be aborted. */
```

The ADR register located at page3 04H of the core controller is used as a temporary register for EEPROM read/write. When the EEPROM load-back sequence specified above is performed, the content of the specified address will be overwritten by the new data. Note that since the EEPROM is word-aligned, each time the sequence is performed one word of data is modified. The address range available is from 00H to ffH. To make sure that the EEPROM is written correctly, the programmer can use the following read-check process to read a word from a specified address in the EEPROM.

```
write (EEAR, EOS = 1 EW/ER = 0);
write (ADR, address);
wait (  );
repeat (
        read(EEAR, EOS);
        ) until (EOS = 0);
read(ADR);          /* read word data */
/* The entire sequence should be consecutive or the process will be aborted. */
```

Note that data will be kept in the ADR until they are updated. That is, the data can be read out any time afterwards unless new data have been written.

SRAM Physical Map

When an EEPROM is used for attribute memory storage, the 32K byte SRAM has two roles in the PENTIC+ design: the first 16K bytes of SRAM serve as an Ethernet buffer ring, while the remainder is used for temporary storage of Ethernet IDs and CIS storage (if EECS/$\overline{FCS}$ is pulled low). The detailed physical mapping of the SRAM memory is shown in the table below. When a flash memory is used, only a 16K byte SRAM is needed to serve as the Ethernet ring buffer.

SRAM Physical Address	EECS/$\overline{FCS}$ pull low	EECS/$\overline{FCS}$ pull high
0000H- 3FFFH	Ethernet Buffer	Ethernet Buffer
4000H	ID0	Unused
4001H	ID1	
4002H	ID2	
4003H	ID3	
4004H	ID4	
4005H	ID5	
4006H	Board Type (05H)	
4007H	Checksum	
4008H- 400DH	-	
400EH	57H	
400FH	57H	
4010H- 41FBH	CIS	
41FCH- 7FFFH	-	

Note that if EECS/$\overline{FCS}$ is pulled low, the CIS is stored in the SRAM starting at address 4010H. The length of the CIS depends on the word count specified in the first byte of EEPROM. During a power-on reset, the PENTIC+ will load the exact word count specified in the EEPROM rather than read in all bytes in the EEPROM.

The PENTIC+ will automatically translate the address from the host if the host tries to read CIS. It will translate the attribute memory address by assuming that the first CIS byte is stored at 00H of attribute memory, the second CIS byte is stored at 02H, and so forth. Users should assign CIS accordingly, or else the CIS may be lost.

Also note that for auto-load information write protection, the PENTIC+ will ignore any write operation above 4000H of SRAM. If it is necessary to change the settings, users should do so by writing the flash memory or EEPROM.

Minimal System Design

A low-cost, dedicated LAN card can be designed using the PENTIC+ chip, a 32K x 8 SRAM, a serial EEPROM (93C66/93CS66), and a pig tail for the network interface MAU, along with certain other peripheral components. The following is a sample CIS table that can be used with this minimal system design:

```
01 03 dc 03 ff
17 03 5b 09 ff
1a 05 01 01 e0 1f  0f
1b 13 c1 c1 7d 19 55 15 26 00 33 43 16 45 70 ff ff 48 40 00 00
14 00
f0 09 'WinICard' ff
21 02 06 03
20 04 u00 u01 u02 u03
15 14 04 01 u04 u05 u06 u07 u08 u09 u10 u11 u12 u13 u14 u15 u16 u17 u18 u19 00 ff
ff ff
```

FLASH MEMORY ACCESS

The flash access and the buffer SRAM share the same memory support bus. The address pins of the flash memory are directly connected to MSA bus and data are accessed through the MSD bus. EECS/$\overline{FCS}$ is active low if it is pulled high and the attribute memory is accessed in the range 00000H to 03FFFH or the common memory is accessed in the range 04000H to 1FFFFH. Note that CFB.FWE should be set to 1 before a flash write command is issued.

I/O MODE OPERATION

The I/O mode provides two DMA channels for system access. The remote DMA moves data between system memory space and local memory space. The local DMA moves data between the FIFO of the SLCT and local memory space. However, since the SLCT can handle local DMA operations without system intervention (refer to the data sheet for the SLCT), the system has to perform only remote DMA reads/writes.

In a transmit operation, the data should first be moved from the system to local buffer memory. This is simply an "OUT" command on the PC. Then the system orders the SLCT to start transmission, and the local DMA starts to move data from buffer memory to the transmit FIFO for transmission.

In a receive operation, the local DMA moves received data from the receive FIFO to the buffer and asserts $\overline{IREQ}$ to the system when the buffer ring needs to be serviced. The system must move data

out before the buffer ring overflows. This is done through a remote DMA read operation, which is simply a "IN" command on the PC.

SHARED MEMORY MODE OPERATION

In this mode, the local memory is mapped as part of the system memory. When it requires data transmission, the host fills the transmit buffer SRAM by a memory move operation and then issues a transmit command to the PENTIC+. When it receives data, the PENTIC+ will generate an interrupt to the host by asserting $\overline{\text{IREQ}}$ when one or more packets have been received. The PENTIC+ will then place the packets into the shared memory. The host should check the shared memory and remove the data before the buffer ring overflows.

Bus arbitration is performed between the host and LCE core for shared memory usage. When memory accesses are issued, the arbiter will grant the bus master an acknowledge signal, which is a BACK to the LCE or a $\overline{\text{WAIT}}$ signal to the host. There is no predefined priority in the PENTIC+; bus arbitration is performed on a first-come, first-served basis.

To implement the shared memory mode, the PENTIC+ uses memory mapping register A (MMA) and memory mapping register B (MMB) for memory mapping control. Since the PENTIC+ will operate in 16-bit shared memory operation at shared memory base address 00000H only, 0s should be written to MMB and bit 0 to 5 of MMA. The contents of the MMA are described below.

MMA (Memory Mapping Register A)

MMA is used for memory enable and software reset. It is located in I/O space, 00H, and can be accessed only in shared memory mode.

Access Address: IOBASE + 00H

Access Type: write-only

BIT	SYMBOL	DESCRIPTION
0-5	-	Reserved. Should be set to 0.
6	MEN	If this bit is high, the buffer memory may be accessed by the system; if it is low, the buffer memory access is disabled. This bit is 0 at power-on.
7	SRESET	A shared memory mode software reset is issued when a 1 is written to this bit. Writing a 0 to this bit will clear the software reset. This bit is 0 at power-on.

AUTO MEDIA-SWITCHING FUNCTION

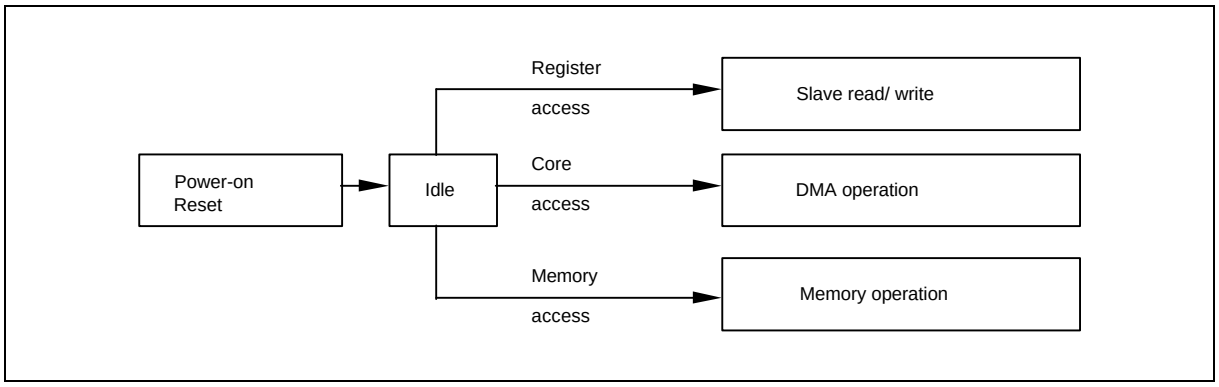
The PENTIC+ also provides a user-friendly auto media-switching function. If the PENTIC+ is configured at the TPI, link checking is enabled, and the UTP link is broken, the PENTIC+ will detect the link status and switch to the BNC port immediately. After the UTP link is repaired, the PENTIC+ will detect the good link and switch back to the TPI again.

If, however, the PENTIC+ is not configured at the TPI or link checking is disabled, the auto media-switching function will be disabled.

BUS ARBITRATION AND STATE DIAGRAM

The PENTIC+ handles bus arbitration automatically. It can operate in four modes: idle state, slave read/write mode, DMA mode, and shared memory mode. The PENTIC+ controls the on-board devices by decoding these modes.

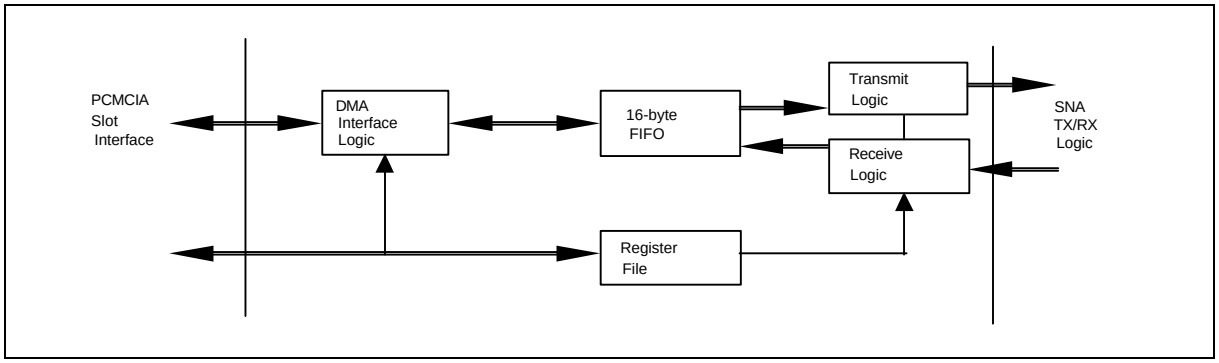
At power-on, the PENTIC+ is in idle mode. If a register read/write command is issued, the PENTIC+ enters the slave read/write mode. If a local DMA or remote DMA (I/O mode only) is initiated by the PENTIC+ core coprocessor, the PENTIC+ enters DMA mode. A memory command will place the PENTIC+ in memory mode. At any given time, the PENTIC+ can be in only one state. The PENTIC+ handles state changes automatically. However, two events, such as a DMA command and a memory command, may be requested at the same time; in this case, the PENTIC+ allocates the bus on a first-come, first-served basis. No predefined priority is set within the PENTIC+.



In cases where the system has no authority on the requested bus, the PENTIC+ will drive the $\overline{WAIT}$ pin low so that the system can insert wait states. After the PENTIC+ has released the bus authority, $\overline{WAIT}$ is deasserted to instruct the system to stop inserting wait states.

SLCT CORE FUNCTION

The SLCT core coprocessor has five major logic blocks that control Ethernet operations: the register files, transmit logic, receive logic, FIFO logic, and DMA logic. The relationship between these blocks is depicted in the following block diagram.



Core Register Files

The register files of the SLCT can be accessed by means of IO commands. The PENTIC+ should be in slave mode when the system accesses the register files. The command register (CR) determines the page number of the register file, while the system address HA<0:4> selects one register address from 01H to 0FH (I/O mode) or from 10H to 1FH (shared memory mode). The PCMCIA $\overline{\text{IORD}}$ and $\overline{\text{IOWR}}$ are the read/write commands used to activate the I/O operations. Refer to the W89C90 data sheet for more detailed information on the registers.

DMA Interface Logic

In I/O mapping mode, the SLCT provides two types of DMA operations, local DMA and remote DMA. In shared memory mode, only local DMA is available.

Local DMA

The local DMA transfers data from/to the on-board buffers. To perform data reception or transmission from/to remote nodes in the network, data must be moved from/to the FIFO. To enhance the efficiency of the transmission, the local DMA transfers data in batches: data are first collected and then moved in a batch. Up to 12 bytes of data can be moved in each transfer. This scheme reduces time wasted in requesting the bus.

A local DMA begins by requesting the local bus. If the local bus is available to the SLCT core, the bus arbiter inside the PENTIC+ responds at once by asserting the bus acknowledge (BACK, refer to LCE); if, on the other hand, the bus is currently authorized to another device, the arbiter will not assert the bus acknowledge and the SLCT must wait. Note that this sequence will not affect the host system or system bus signals. After each batch of data is transferred, the SLCT checks the FIFO threshold levels to determine if another batch transfer should be requested.

Remote DMA

A remote DMA can be performed only in I/O mode. The remote DMA moves data between the host and the local buffers. Unlike a local DMA, the remote DMA is word-wide: the remote DMA operation transfers one word each time.

Since a remote DMA is simply a system I/O operation, it sometimes affects the system bus. If the remote DMA is interleaved with other devices, $\overline{\text{WAIT}}$ is asserted to force the system to insert wait states. The PENTIC+ will automatically handle any arbitration necessary.

FIFO Logic

The SLCT has a 16-byte FIFO, which acts as an internal buffer to compensate for differences in the transmission/reception speed of different DMAs. The FIFO has FIFO threshold pointers to determine the level at which it should initiate a local DMA. The threshold levels, Which are different for reception and transmission, are defined in the DCR register.

The FIFO logic also provides FIFO overrun and underrun signals for network management purposes. If received packets are flooding into the FIFO but the SLCT still does not have bus authority, the FIFO may be overrun. On the other hand, if a transmission begins before data are fed into the FIFO, it may be underrun. Either case results in a network error. FIFO overruns and underruns can be prevented by changing the values of the FIFO thresholds.

Normally, the data in the FIFO cannot be read; reading FIFO data during normal operation may cause $\overline{\text{WAIT}}$ to be asserted and the system to hang. In loopback mode, however, the SLCT allows FIFO data to be read by byte in order to check the correctness of the loopback operation.

Receive Logic

The receive logic is responsible for receiving the serial network data and packing the data in byte/word sequence. The receive logic thus has serial-to-parallel logic in addition to network detection capability.

The PENTIC+ accepts both physical addresses and group addresses (multicast and broadcast addresses). The SLCT extracts the address field from the serial input data. It then determines if the address is acceptable according to the configurations defined in the Receive Configuration Register (RCR). If the address is not acceptable, the packet reception is aborted. If the address is acceptable, the data packet is sent to the serial-to-parallel logic before being fed into the FIFO.

After receiving a data packet, the SLCT automatically adds four bytes of data receive status, next packet pointer, and two bytes of receive byte count into the FIFO for network management purposes. The receive status contains the status of the incoming packet, so that the system can determine if the packet is desired. The next packet pointer points to the starting address of the next packet in the local receive ring. The receive byte count is the length of the packet received by the SLCT. Note that the receive byte count may be different from the "length" field specified in the Ethernet packet format. These four bytes of data will be transferred to the local buffer with the last batch of the local DMA. However, these four bytes are stored at the first four addresses of the packet.

Transmit Logic

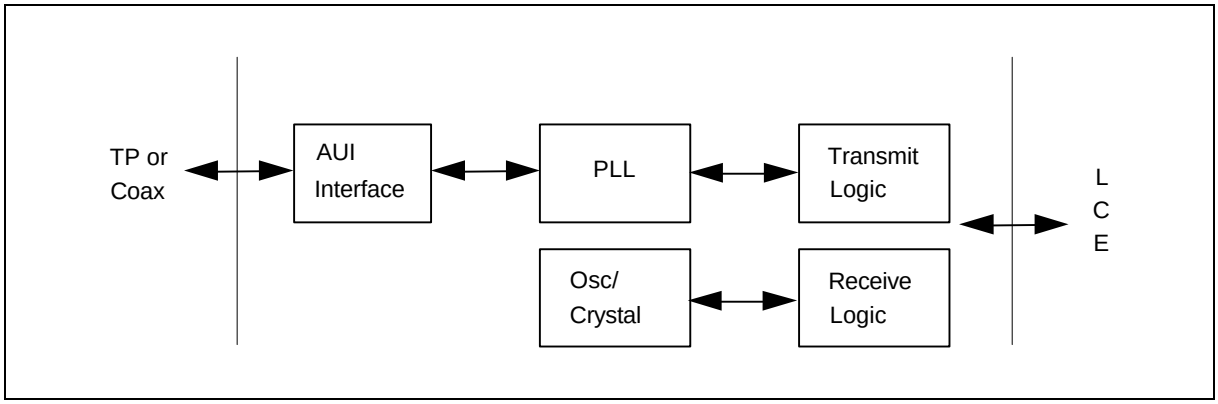
The SLCT must be filled before transmission may begin. That is, the local DMA read must begin before the SLCT starts transmission. The SLCT first transmits 62 bits of preamble, then two bits of SFD, and then the data packet. The parallel-to-serial logic serializes the data from the FIFO into a data packet. After the data packet, the SLCT optionally adds four bytes of cyclic redundancy code (CRC) to the tail of the packet.

A protocol PLA determines the network operations of the PENTIC+. Collision detection, random back-off, and auto retransmit are implemented in the transmit logic. The protocol PLA ensures that the PENTIC+ follows the IEEE 802.3 protocol.

SNA Module

The PENTIC+ also contains a serial network adaptor (SNA), which adapts the non-return-to-zero (NRZ) used in the core processor and host system to Manchester coded network symbols. Two kinds of interfacing signals are provided in the PENTIC+: an AUI interface for Ethernet and a coaxial

interface for Cheapernet. The SNA contains three blocks: a phase locked loop (PLL), a Manchester encoder/decoder, and a collision decoder as well as crystal/oscillator logic.



The Manchester encoder/decoder handles code interpretation between NRZ signals and Manchester coded signals. The PLL locks the receiving signals with an internal voltage control oscillator (VCO) so that network noise can be eliminated before the signals enter the core coprocessor. The collision decoder detects whether a collision has occurred on the network. The oscillator logic supplies the PENTIC+ with the required 20 MHz clock. This clock also supplies the SNA clocking system.

TWISTED PAIR INTERFACE MODULE FUNCTION

Transmit Driver

There are two signals for data transmission: the true and complement Manchester differential data (TXO+/-). These two signals are resistively combined to form a pre-equalized differential pair, which is then passed to the twisted-pair cable via a transmitter filter and an optional common mode choke.

Smart Squelch

The main function of this block is to determine when valid data are present on the differential receiving inputs (RXI+/-). To ensure that impulse noise on the medium will not be taken to be valid data, this circuit adopts a combination of amplitude and timing measurements to determine the validity of the input signals. To qualify incoming data, the smart squelch circuitry monitors the signals for three peaks of alternating polarity that occur within a 400 nS window. Once this condition has been satisfied, the squelch level is reduced to minimize the noise effect and the chances of causing premature Start Of Idle (SOI) pulse detection. If the receiver detects activity on the receive line while packets are being transmitted, incoming data are qualified on five peaks of alternating polarity so as to prevent false collisions caused by impulse noise. The squelch function returns to its squelch state under any of the following conditions:

- A normal SOI signal
- An inverted SOI signal
- A missing SOI signal

A missing SOI signal is assumed when no transitions have occurred on the receiver for 175 nS after a packet has arrived. In this case, a normal SOI signal is generated and appended to the data.

Collision Detection

The collision detection logic determines when transmit and receive signals occur simultaneously on the twisted pair cable. Collisions will not be reported when the device is in a link-fail state. The collision signal is also generated when the transceiver has detected a jabber condition or when the SQE test is being performed.

SQE Test

The Signal Quality Error (SQE) test is used to test the collision signaling circuitry in the twisted-pair transceiver module. After each packet transmission, an SQE signal is sent to the SLCT. The SLCT expects this signal and will flag an error if it does not exist.

Jabber

The jabber timer monitors the transmitter and disables the transmission if the transmitter is active for greater than 26.2 mS. The jabber will re-enable the transmitter after the SLCT has been idle for at least 420 mS.

Link Integrity

During periods of inactivity, link pulses are generated and received by both MAUs at either end of the twisted pair to ensure that the cable has not been broken or shorted. A positive, 100 nS link integrity signal is generated by the twisted-pair transceiver and transmitted on the twisted pair cable every 13 mS during periods of no transmission activity. The PENTIC+ assumes a link-good state if it detects valid link pulse activity on the twisted-pair transceiver receive circuit. If neither receive data nor a link pulse (positive or negative) is detected within 105 mS, the PENTIC+ enters a link-fail state. When a link-fail condition occurs, four consecutive positive link pulses (or eight negative link pulses) must be received before a link-good condition is assumed.

LCE CORE REGISTERS

This section lists the access addresses and access types of the LCE core registers. Refer to the W89C90 or W89C901 data sheet for more detailed information.

Page 0 Address Assignments (PS1 = 0, PS0 = 0)

RA0-3	READ	WRITE
00	Command (CR)	Command (CR)
01	Current Local DMA Address 0 (CLDA0)	Page Start Register (PSTART)
02	Current Local DMA Address 1 (CLDA1)	Page Stop Register (PSTOP)
03	Boundary Pointer (BNRY)	Boundary Pointer (BNRY)
04	Transmit Status Register (TSR)	Transmit Page Start Address (TPSR)
05	Number of Collisions Register (NCR)	Transmit Byte Count Register 0 (TBCR0)
06	FIFO (FIFO)	Transmit Byte Count Register 1 (TBCR1)
07	Interrupt Status Register (ISR)	Interrupt Status Register (ISR)
08	Current Remote DMA Address 0 (CRDA0)	Remote Start Address Register 0 (RSAR0)

Page 0 Address Assignments (PS1 = 0, PS0 = 0), continued

RA0-3	READ	WRITE
09	Current Remote DMA Address 1 (CRDA1)	Remote Start Address Register 1 (RSAR1)
0A	Reserved	Remote Byte Count Register 0 (RBCR0)
0B	Reserved	Remote Byte Count Register 1 (RBCR1)
0C	Received Status Register (RSR)	Receive Configuration Register (RCR)
0D	Tally Counter 0 (Frame Alignment Errors) (CNTR0)	Transmit Configuration Register (TCR)
0E	Tally Counter 1 (CRC Errors)(CNTR1)	Data Configuration Register (DCR)
0F	Tally Counter 2 (Missed Packet Errors) (CNRT2)	Interrupt Mask Register (IMR)

Page 1 Address Assignments (PS1 = 0, PS0 = 1)

RA0-3	READ	WRITE
00	Command (CR)	Command (CR)
01	Physical Address Register 0 (PAR 0)	Physical Address Register 0 (PAR 0)
02	Physical Address Register 1 (PAR 1)	Physical Address Register 1 (PAR 1)
03	Physical Address Register 2 (PAR 2)	Physical Address Register 2 (PAR 2)
04	Physical Address Register 3 (PAR 3)	Physical Address Register 3 (PAR 3)
05	Physical Address Register 4 (PAR 4)	Physical Address Register 4 (PAR 4)
06	Physical Address Register 5 (PAR 5)	Physical Address Register 5 (PAR 5)
07	Current Page Register (CURR)	Current Page Register (CURR)
08	Multicast Address 0 (MAR 0)	Multicast Address 1 (MAR 0)
09	Multicast Address 1 (MAR 1)	Multicast Address 1 (MAR 1)
0A	Multicast Address 2 (MAR 2)	Multicast Address 2 (MAR 2)
0B	Multicast Address 3 (MAR 3)	Multicast Address 3 (MAR 3)
0C	Multicast Address 4 (MAR 4)	Multicast Address 4 (MAR 4)
0D	Multicast Address 5 (MAR 5)	Multicast Address 5 (MAR 5)
0E	Multicast Address 6 (MAR 6)	Multicast Address 6 (MAR 6)
0F	Multicast Address 7 (MAR 7)	Multicast Address 7 (MAR 7)

Page 2 Address Assignments (PS1 = 1, PS0 = 0)

RA0-3	READ	WRITE
00	Command (CR)	Command (CR)
01	Page Start Register (PSTART)	Current Local DMA Address 0 (CLDA0)
02	Page Stop Register (PSTOP)	Current Local DMA Address 1 (CLDA1)
03	Remote Next Packet Pointer	Remote Next Package Pointer
04	Transmit Page Start Address (TPSR)	Reserved
05	Local Next Packet Pointer	Local Next Packet Pointer
06	Address Counter (Upper)	Address Counter (Upper)
07	Address Counter (Lower)	Address Counter (Lower)
08	Reserved	Reserved
09	Reserved	Reserved
0A	Reserved	Reserved
0B	Reserved	Reserved
0C	Receive Configuration Register (RCR)	Reserved
0D	Transmit Configuration Register (TCR)	Transmit Configuration
0E	Data Configuration Register (DCR)	Reserved
0F	Interrupt Mask Register (IMR)	Reserved

Note: Page 2 registers should be accessed only for diagnostic purposes. They should not be modified during operation. Page 3 should never be modified.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_S	-55	150	°C
Supply Voltage	V_{DD}	-0.5	7.0	V
Input Voltage	V_{IN}	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5	V_{DD}+0.5	V
Lead Temperature (soldering 10 seconds maximum)	T_L	-	250	°C
ESD Tolerance	ESD	2K	-	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

Power Supply:

(V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0° C to 70° C)

PARAMETER		SYM.	CONDITIONS	MIN.	MAX.	UNIT
Average Idle Supply Current	Note 1	I_{AVI}	V_{DD} = 5.25V	-	150	mA
Average Transmit Supply Current	Note 2	I_{AVT}	V_{DD} = 5.25V	-	250	mA

Notes:

1. X1 = 20 MHz, V_{IN} = V_{CC} or GND.
2. X1 = 20 MHz, normal transmitting operation.

Digital:

(V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0° C to 70° C)

PARAMETER	SYM.	CONDITIONS	MIN.	MAX.	UNIT
Low Input Voltage	V_{IL}		V_{SS}-0.5	0.8	V
High Input Voltage	V_{IH}		2.0	V_{DD}+0.5	V
Low Output Voltage	V_{OL}	V_{DD} = 4.75V, I_{OL} = I_{OL-MIN}	-	0.4	V
High Output Voltage	V_{OH}	V_{DD} = 4.75V, I_{OH} = I_{OL-MAX}	2.4	-	V
Low Output Sink Current	I_{OL1}		4		mA
High Output Drive Current	I_{OH1}		-	-4	mA
Low Output Sink Current*	I_{OL2}		2	-	mA
High Output Drive Current*	IOH2		-	-2	mA
Output 3-State Leakage Current	IOTR	V_{DD} = 5.25V	-	10	µA

* These are the parameteres for MSD0-7 and MSA0-15.

AUI:

(V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0° C to 70° C)

PARAMETER	SYM.	CONDITIONS	MIN.	MAX.	UNIT
Differential Output Voltage (TX+/-)	V_{DD}	With test load	+/-550	+/-1200	mV
Differential Output Voltage Imbalance (TX+/-)	V_{OB}	With test load	-	40	mV
Undershoot Voltage (TX+/-)	V_U	With test load	-	100	mV
Differential Squelch Threshold (CD+/-, RX+/-)	V_{DS}		-175	-300	mV
Differential Input Common Mode Voltage (CD+/-, RX+/-)	V_{CM}		2.0	4.0	V

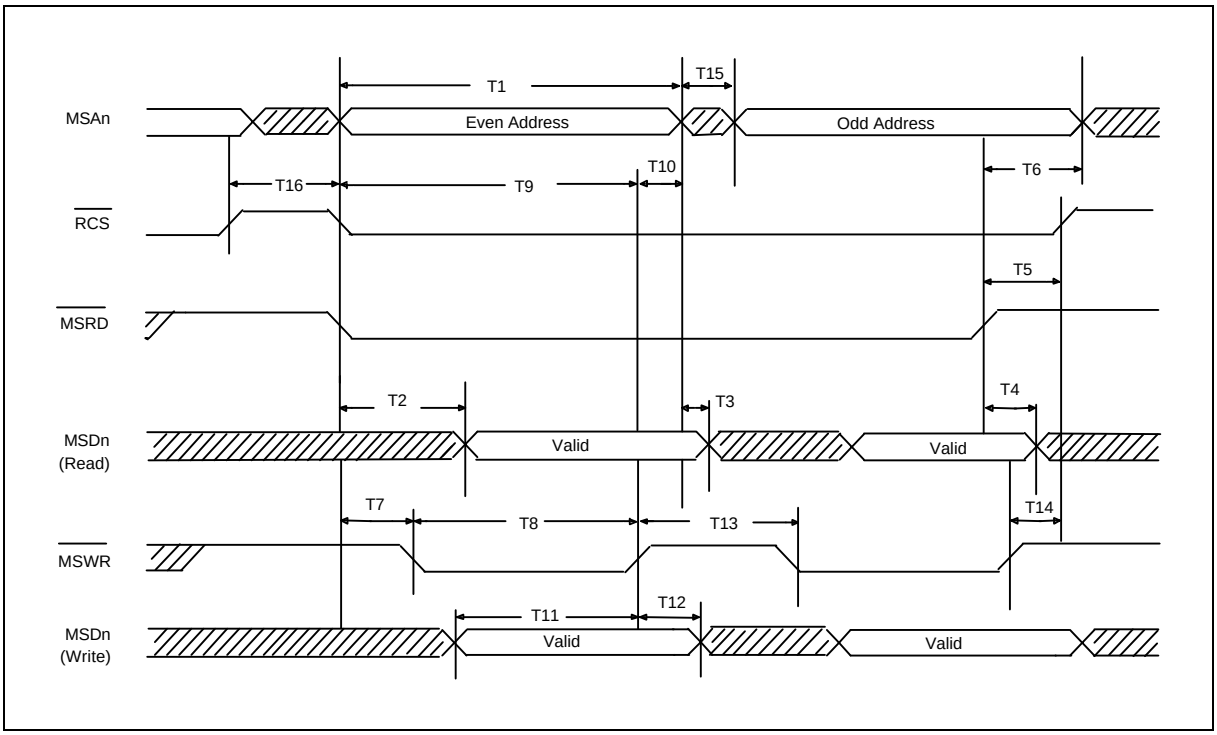
Twisted Pair:

(V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0° C to 70° C)

PARAMETER	SYM.	CONDITIONS	MIN.	MAX.	UNIT
RXI+/- Differential Input Resistance	R_{TI}		3	-	KΩ
RXI+/- Open Circuit Input Voltage (bias)	V_{TIB}		-2.75	V_{DD}-1.0	V
RXI+/- Differential Input Voltage Range	V_{TIV}	V_{DD} = 5V	-3.1	3.1	V
RXI+/- Positive Squelched Threshold	V_{TPS}		300	585	mV
RXI+/- Negative Squelched Threshold	V_{TNS}		-585	-300	mV
RXI+/- Positive Unsquelched Threshold	V_{TPU}		200	350	mV
RXI+/- Negative Unsquelched Threshold	V_{TNU}		-350	-200	mV
TXO+/- Differential Output Voltage	V_{TO}	With test load	2.2	2.8	V

SWITCHING CHARACTERISTICS

Memory Support Bus Access (SRAM Access)



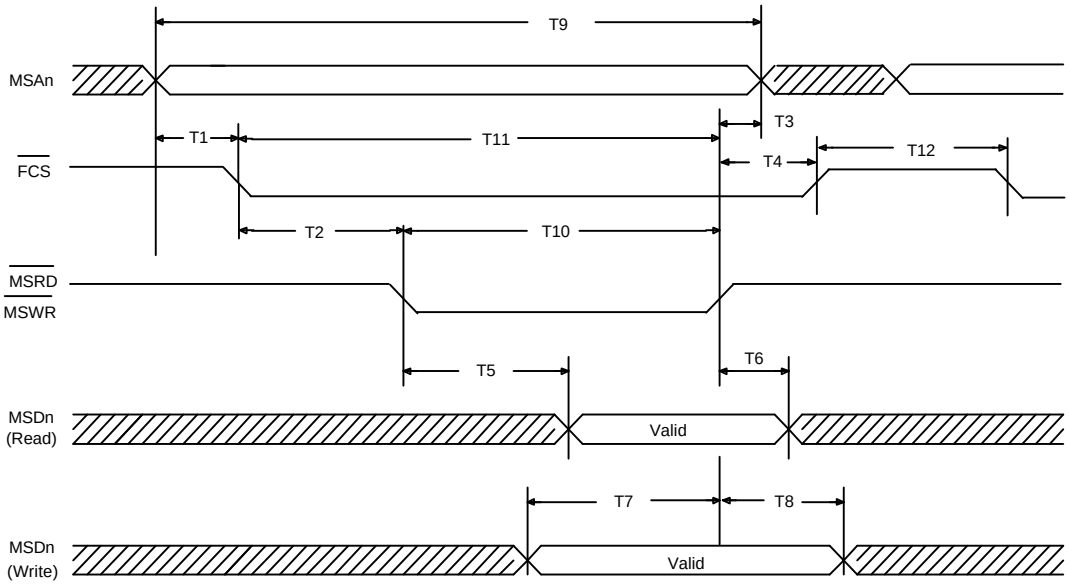
SRAM (upper and lower values are for 70 nS and 15 nS SRAMs, respectively)

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T1	Read cycle time.	70 15	- -	nS
T2	MSA0-15 valid to MSD0-7 read data valid.	- -	70 15	nS
T3	MSD0-7 read data hold valid from MSA0-15 change.	5 3	- -	nS
T4	MSD0-7 read data hold from $\overline{\text{MSRD}}$ deasserted.	0 0	- -	nS
T5	$\overline{\text{RCS}}$ held valid after $\overline{\text{MSRD}}$ deasserted.	5 3	- -	nS
T6	MSA0-15 held valid after $\overline{\text{MSRD}}$ deasserted.	5 3	- -	nS
T7	$\overline{\text{RCS}}$ asserted to $\overline{\text{MSWR}}$ asserted	0 0	- -	nS
T8	$\overline{\text{MSWR}}$ pulse width	60 15	- -	nS
T9	$\overline{\text{RCS}}$ asserted to $\overline{\text{MSWR}}$ deasserted.	60 15	- -	nS
T10	MSA0-15 held valid after $\overline{\text{MSWR}}$ deasserted.	5 3	- -	nS
T11	MSD0-7 write data setup before $\overline{\text{MSWR}}$ asserted.	35 10	- -	nS
T12	MSD0-7 write data hold after $\overline{\text{MSWR}}$ deasserted.	5 3	- -	nS
T13	Even byte $\overline{\text{MSWR}}$ deasserted to odd byte $\overline{\text{MSWR}}$ asserted. (see note)	10 5	- -	nS
T14	$\overline{\text{RCS}}$ held valid after $\overline{\text{MSWR}}$ deasserted.	5 3	- -	nS
T15	Even byte address invalid to odd byte address valid. (see note)	0 0	- -	nS
T16	Command recovery time.	30 10	- -	nS

Note: This timing is invalid for byte access, e.g, attribute memory reading on SRAM image.

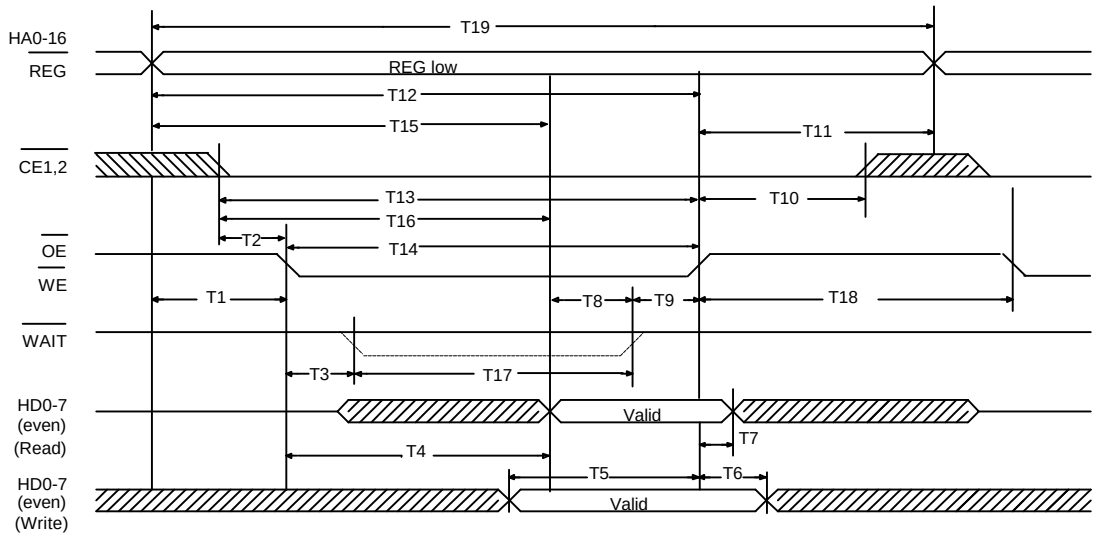
Flash Memory

Memory Support Bus Access (Flash Access)



SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T1	MSA0-16 valid to $\overline{FCS}$ asserted.	0	-	nS
T2	$\overline{FCS}$ asserted to $\overline{MSRD}$, $\overline{MSWR}$ asserted.	20	-	nS
T3	MSA0-16 held valid after $\overline{MSRD}$, $\overline{MSWR}$ deasserted.	5	-	nS
T4a	$\overline{FCS}$ held valid after $\overline{MSRD}$ deasserted.	0	-	nS
T4b	$\overline{FCS}$ held valid after $\overline{MSWR}$ deasserted.	5	-	nS
T5	$\overline{MSRD}$ asserted to read data valid.	-	60	nS
T6	Read data hold from $\overline{MSRD}$ deasserted.	0	-	nS
T7	Write data setup to $\overline{MSWR}$ deasserted.	55	-	nS
T8	Write data hold from $\overline{MSWR}$ deasserted.	15	-	nS
T9	Access cycle time	150	-	nS
T10	Write pulse width	55		nS
T11	$\overline{FCS}$ asserted to $\overline{MSWR}$ deasserted	75	-	nS
T12a	Write recovery time before read	6	-	µS
T12b	Read recovery time before write	0	-	µS
T12c	Consecutive same commands interval	20	-	nS

Attribute Memory Access



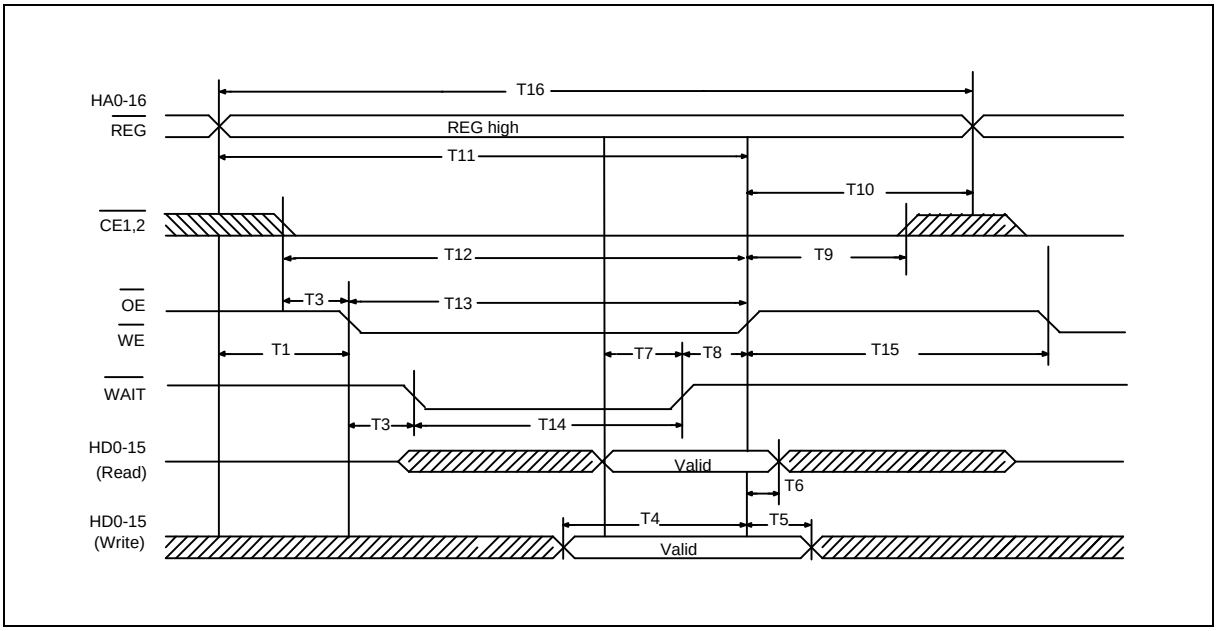
SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T1	HA0-16, $\overline{REG}$ valid to $\overline{OE}$, $\overline{WE}$ asserted	30	-	nS
T2	$\overline{CE1,2}$ asserted to $\overline{OE}$, $\overline{WE}$ asserted	0	-	nS
T3	$\overline{OE}$, $\overline{WE}$ asserted to $\overline{WAIT}$ asserted	-	35	nS
T4	$\overline{OE}$ asserted to HD0-7 read data valid (see note)	-	150	nS
T5	HD0-7 write data setup before $\overline{WE}$ deasserted	80	-	nS
T6	HD0-7 write data hold from $\overline{WE}$ deasserted	30	-	nS
T7	HD0-7 read data disable from $\overline{OE}$ deasserted	-	100	nS
T8	Read data setup before $\overline{WAIT}$ deasserted	0	-	nS
T9	$\overline{WAIT}$ deasserted to $\overline{OE}$, $\overline{WE}$ deasserted	0	-	nS
T10	$\overline{CE1,2}$ hold valid from $\overline{OE}$, $\overline{WE}$ deasserted	20	-	nS
T11	HA0-16, $\overline{REG}$ hold valid from $\overline{OE}$, $\overline{WE}$ deasserted	20	-	nS
T12	HA0-16, $\overline{REG}$ setup to $\overline{WE}$ deasserted	180	-	nS

Attribute Memory Access, continued

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T13	$\overline{CE1,2}$ asserted to $\overline{WE}$ deasserted	180	-	nS
T14	$\overline{WE}$ pulse width	150	-	nS
T15	HA0-16, $\overline{REG}$ valid to read data valid (see note)	-	300	nS
T16	$\overline{CE1,2}$ asserted to read data valid (see note)	-	300	nS
T17	$\overline{WAIT}$ pulse width	-	12	µS
T18a	$\overline{OE}$ deasserted to next $\overline{WE}$ asserted	10	-	nS
T18b	$\overline{WE}$ deasserted to next $\overline{OE}$ asserted	10	-	nS
T19a	Read cycle time	300	-	nS
T19b	Write cycle time	250	-	nS

Note: These timings are specified when the PENTIC+ does not assert $\overline{WAIT}$.

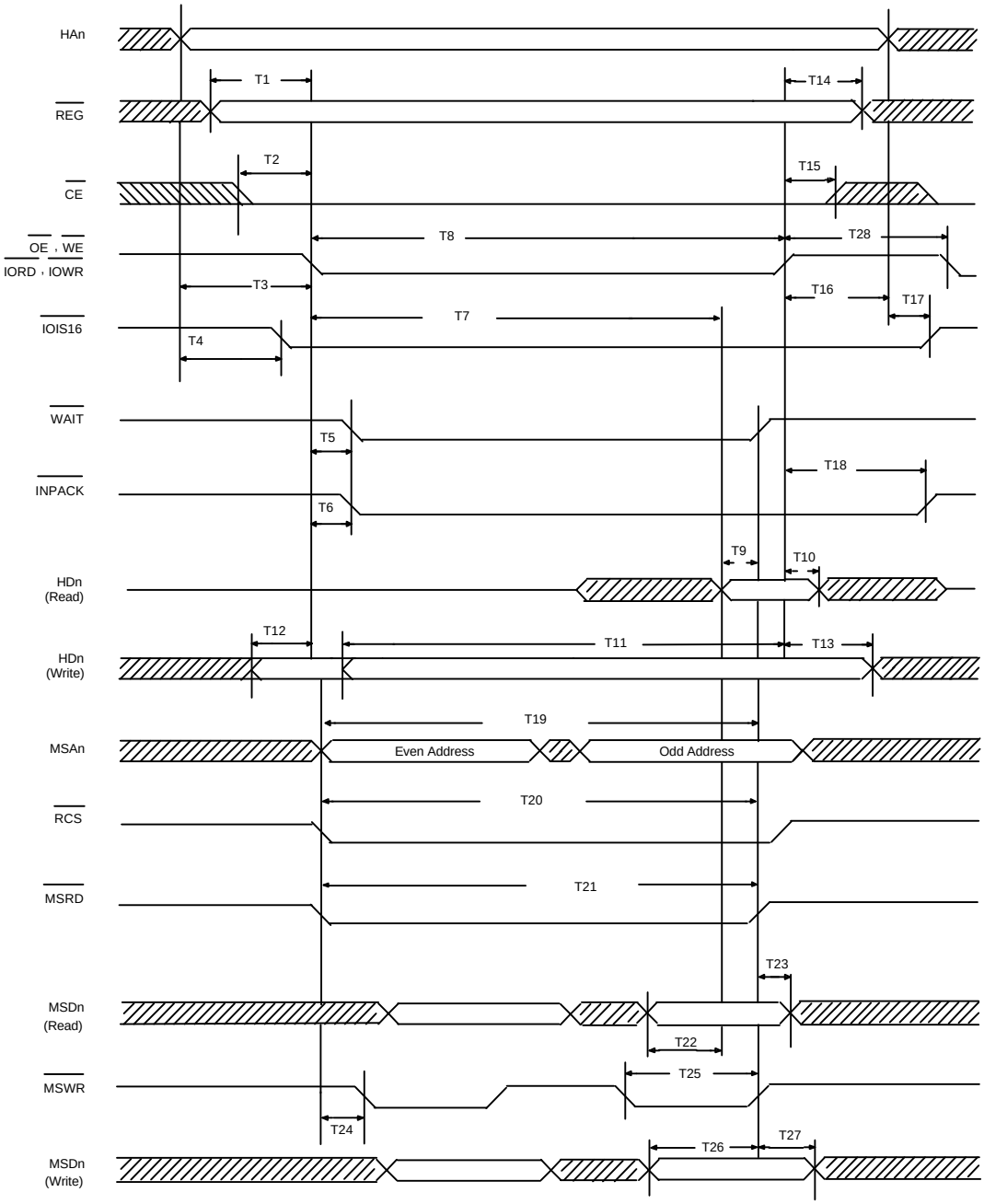
Common Memory Access



Common Memory Access, continued

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T1	HA0-16, $\overline{REG}$ valid to $\overline{OE}$, $\overline{WE}$ assert.	20	-	nS
T2	$\overline{CE1,2}$ assert to $\overline{OE}$, $\overline{WE}$ assert.	0	-	nS
T3	$\overline{OE}$, $\overline{WE}$ assert to $\overline{WAIT}$ asserts.	-	35	nS
T4	HD0-15 write data setup before $\overline{WE}$ deasserts.	50	-	nS
T5	HD0-15 write data hold from $\overline{WE}$ deasserts.	20	-	nS
T6	HD0-15 read data disable from $\overline{OE}$ deasserts.	-	75	nS
T7	Read data setup before $\overline{WAIT}$ deasserts.	0	-	nS
T8	$\overline{WAIT}$ deasserts to $\overline{OE}$, $\overline{WE}$ deassert.	0	-	nS
T9	$\overline{CE1,2}$ hold valid from $\overline{OE}$, $\overline{WE}$ deassert	20	-	nS
T10	HA0-16, $\overline{REG}$ hold valid from $\overline{OE}$, $\overline{WE}$ deassert	20	-	nS
T11	HA0-16, $\overline{REG}$ setup to $\overline{WE}$ deassert	100	-	nS
T12	$\overline{CE1,2}$ assert to $\overline{WE}$ deassert	100	-	nS
T13	$\overline{WE}$ pulse width	80	-	nS
T14	$\overline{WAIT}$ pulse width	-	12	µS
T15a	$\overline{OE}$ deassert to next $\overline{WE}$ assert	10	-	nS
T15b	$\overline{WE}$ deassert to next $\overline{OE}$ assert	10	-	nS
T16a	Read cycle time	150	-	nS
T16b	Write cycle time	150	-	nS

PCMCIA Bus Slave Access



PCMCIA Bus Slave Access

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T1a	HA0-16 & $\overline{REG}$ valid to $\overline{OE}$, $\overline{WE}$ asserted Note 2	10	-	nS
T1b	HA0-16 & $\overline{REG}$ valid to $\overline{IORD}$, $\overline{IOWR}$ asserted. Note 3	5	-	nS
T2a	$\overline{CE1,2}$ asserted to $\overline{OE}$, $\overline{WE}$ asserted.	0	-	nS
T2b	$\overline{CE1,2}$ asserted to $\overline{IORD}$, $\overline{IOWR}$ asserted.	5	-	nS
T3a	HA0-16 valid to $\overline{OE}$, $\overline{WE}$ asserted.	10	-	nS
T3b	HA0-16 valid to $\overline{IORD}$, $\overline{IOWR}$ asserted.	70	-	nS
T4	HA0-16 valid to $\overline{IOIS16}$ asserted. Note 4	-	35	nS
T5	$\overline{OE}$, $\overline{WE}$, $\overline{IORD}$, $\overline{IOWR}$ asserted to $\overline{WAIT}$ asserted. Note 1	-	35	nS
T6	$\overline{IORD}$ asserted to $\overline{INPACK}$ asserted. Note 8	-	40	nS
T7a	$\overline{IORD}$ asserted to HD0-15 read data valid. Note 6	-	100	nS
T7b	$\overline{OE}$ asserted to HD0-15 read data valid. Note 9	-	50	nS
T8	$\overline{IORD}$, $\overline{IOWR}$ minimum width time.	165	-	nS
T9a	$\overline{WAIT}$ deasserted to HD0-15 memory read data valid. Note 1, 5	-	0	nS
T9b	$\overline{WAIT}$ deasserted to HD0-15 I/O read data valid. Note 1, 5	-	0	nS
T10	HD0-15 read data hold after $\overline{OE}$, $\overline{IORD}$ deasserted.	5	-	nS
T11	HD0-15 write data setup before $\overline{WE}$ deasserted.	40	-	nS
T12	HD0-15 write data setup befor $\overline{IOWR}$ assert.	60	-	
T13a	HD0-15 write data hold after $\overline{WE}$ deasserted.	15	-	nS
T13b	HD0-15 write data hold after $\overline{IOWR}$ deasserted.	30	-	nS
T14a	$\overline{OE}$, $\overline{WE}$ deasserted to $\overline{REG}$ deasserted. Note 7	15	-	nS
T14b	$\overline{IORD}$, $\overline{IOWR}$ deasserted to $\overline{REG}$ deasserted. Note 7	0	-	nS
T15a	$\overline{OE}$, $\overline{WE}$ deasserted to $\overline{CE1,2}$ deasserted.	15	-	nS
T15b	$\overline{IORD}$, $\overline{IOWR}$ deasserted to $\overline{CE1,2}$ deasserted.	20	-	nS
T16a	$\overline{OE}$, $\overline{WE}$ deasserted to HA0-16 deasserted.	15	-	nS

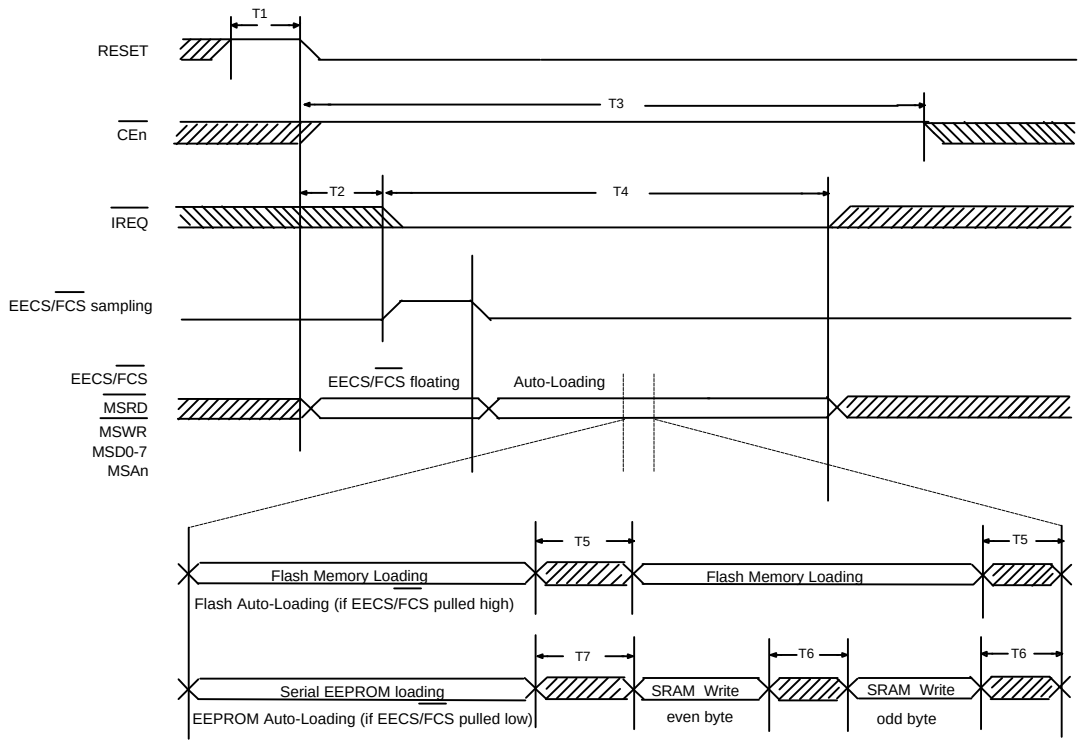
PCMCIA bus slave access, continued

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T16b	$\overline{IORD}$, $\overline{IOWR}$ deasserted to HA0-16 deasserted.	20	-	nS
T17	HA0-16 deasserted to $\overline{IOIS16}$ deasserted. Note 4	-	30	nS
T18	$\overline{IORD}$ deasserted to $\overline{INPACK}$ deasserted.	-	40	nS
T19	MSA0-14 asserted t0 $\overline{WAIT}$ deasserted. Note 1	-	265	nS
T20	$\overline{CE1,2}$ asserted to $\overline{RCS}$ asserted.	-	265	nS
T21	$\overline{OE}$, asserted to $\overline{ROE}$ asserted. Note 2	-	215	nS
T22	MSD odd byte read data valid to HD0-15 read data valid.	-	35	nS
T23a	MSD odd byte read data hold after $\overline{MSRD}$ deasserted.	5	-	nS
T23b	MSD odd byte read data hold after $\overline{MSRD}$ deasserted. Note.10	3	-	nS
T24	MSA0-14 valid to $\overline{MSWR}$ asserted.	0	-	nS
T25	second $\overline{MSWR}$ asserted before $\overline{WAIT}$ deasserted. Note 1	-	140	nS
T26a	MSD write data setup before $\overline{MSWR}$ deasserted.	35	-	nS
T26b	MSD write data setup before $\overline{MSWR}$ deasserted. Note.10	10	-	nS
T27a	MSD write data hold after $\overline{MSWR}$ deasserted.	5	-	nS
T27b	MSD write data hold after $\overline{MSWR}$ deasserted. Note.10	3	-	nS
T28	Command deasserted to next command asserted	150	-	nS

Notes: 1. This is the timing for insert wait states. $\overline{WAIT}$ is asserted if the core cannot service the access immediately; it will hold asserted until the core is ready, causing the system to insert wait states.

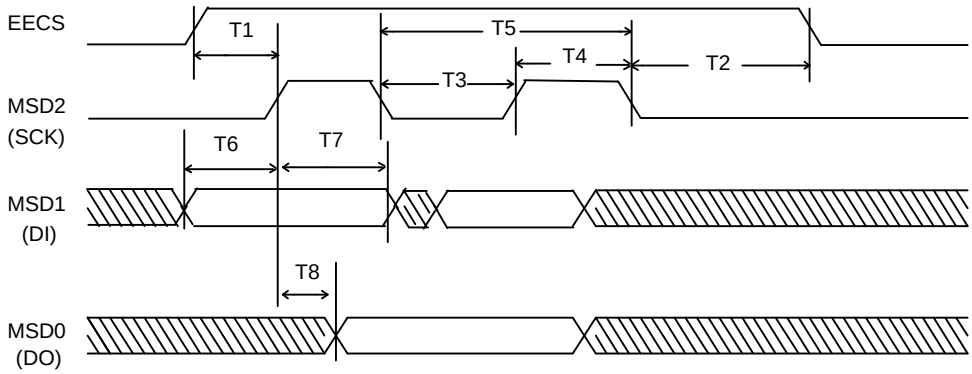
2. This is the timing for shared memory access.
3. This is the timing for I/O access.
4. $\overline{IOIS16}$ is asserted for 16-bit I/O transfers.
5. Read data valid is referenced to $\overline{WAIT}$ when wait states are inserted.
6. If no wait states are inserted, read data valid can be referenced from $\overline{OE}$, $\overline{IORD}$.
7. $\overline{REG}$ is asserted for I/O access and it is deasserted for common memory access.
8. $\overline{INPACK}$ is asserted only for I/O read operation.
9. This is a shared memory access without bus contention.
10. This is the timing for SRAM-15.

H/W Reset and Auto-Initialization Timing



SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T1	Reset pulse width	500	-	nS
T2	Reset deasserted to EECS/$\overline{FCS}$ sampling	400	-	nS
T3	Reset deasserted to $\overline{CE1,2}$ asserted	20	-	mS
T4	Nonvolatile memory auto-load time	-	10	mS
T5	Flash memory auto-reading recovery time	60	-	nS
T6	SRAM image auto-writing recovery time	20	-	nS
T7	EEPROM auto-reading recovery time	50	-	nS

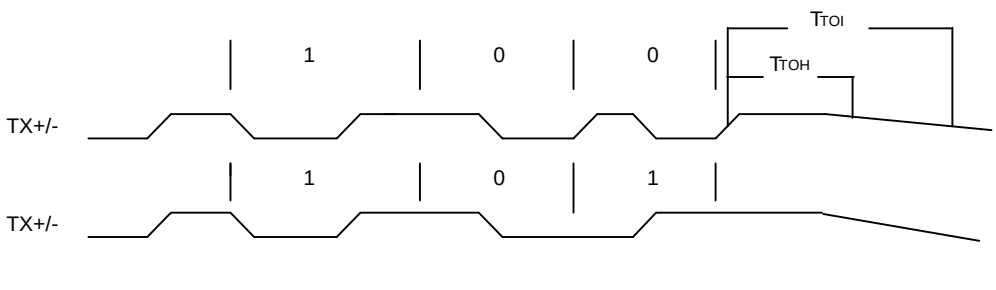
Serial EEPROM Timing



Serial EEPROM Timing

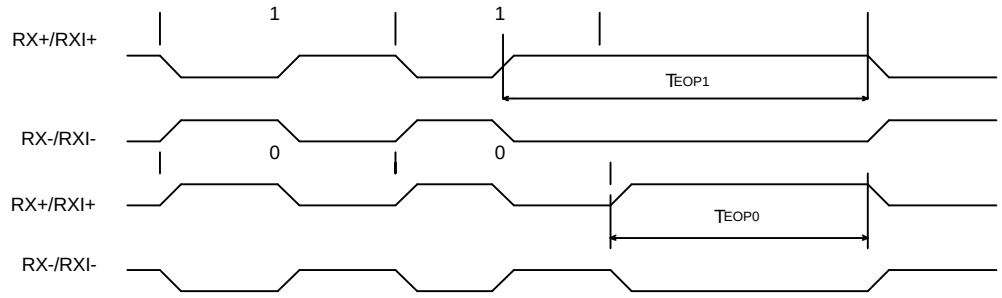
SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T1	EECS asserted to SK	500		nS
T2	EECS hold from SK	0	-	nS
T3	MSD2 OFF time	500	-	nS
T4	MSD2 ON time	500	-	nS
T5	MSD2 clock period	1	-	µS
T6	MSD1 set up time to MSD2 high	500	-	nS
T7	MSD1 hold time from MSD2 high	500	-	nS
T8	MSD0 valid from MSD2 high		500	nS

AUI Transmit Timing (End of Transmit)



SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
TTOH	Transmit Output High Before Idle	200		nS
TTOI	Transmit Output Idle Time		8000	nS

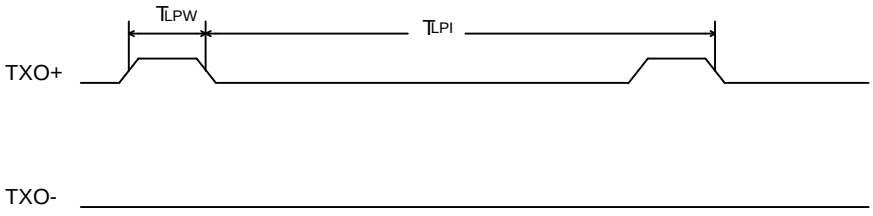
AUI Receive Timing (End of Receive)



SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
TEOP1	End of Packet Received Hold Time after Logic "1"	200		nS
TEOP0	End of Packet Received Hold Time after Logic "0"	200		nS

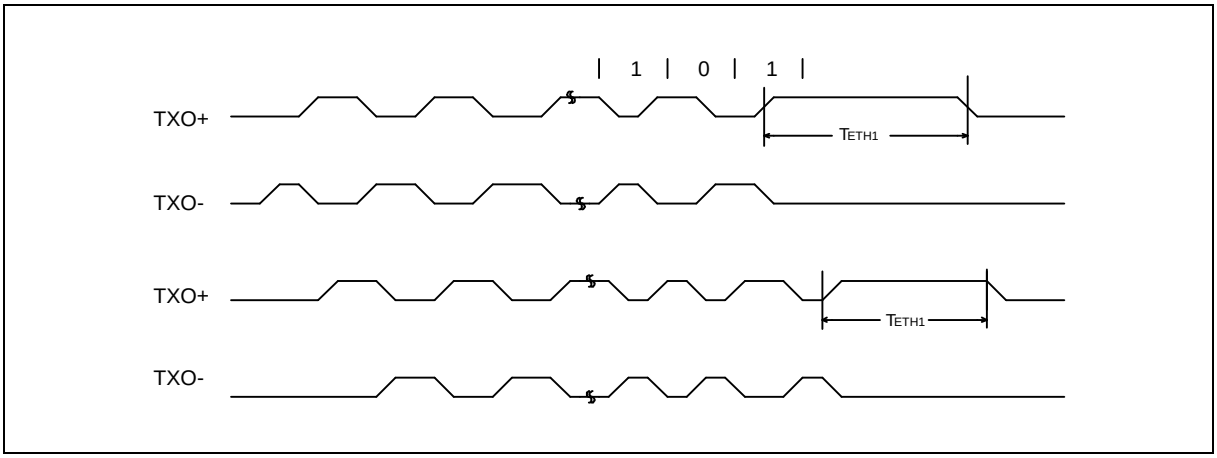
Note: These parameters are specified by design and are not tested.

Link Pulse Timing



SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
TLPI	Link Output Pulse Interval	8	24	mS
TLPW	Link Output Pulse Width	80	120	nS

TPI Transmit Timing (End of Transmit)



SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
TETH1	End of Packet Transmitted Hold Time 1 (TXP/N)	250		nS

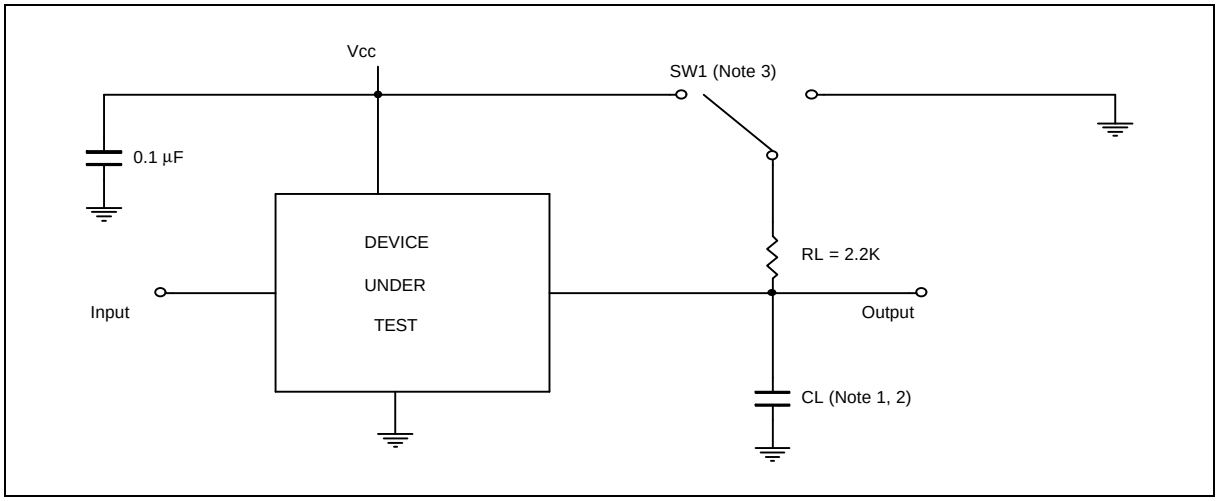
Note: This parameter is specified by design and is not tested.

AC TIMING TEST CONDITIONS

PARAMETER	TEST CONDITIONS
Supply Voltage (VDD/VSS)	5V ± 0.25V
Temperature	25° C/70° C
Input Test Pattern Levels (TTL/CMOS)	GND to 3.0V
Input Rise and Fall Times (TTL/CMOS)	5 nS
Input and Output Pattern Reference Level (TTL/CMOS)	1.3V
Input Waveform Level (Diff)	-350 to -1315 mV
Input and Output Waveform Reference Levels (Diff)	50% Point of the Differential
3-State Reference Levels	Float (V) ± 0.5V

Note: The above specifications are valid only if the mandatory isolations are properly employed and all differential signals are taken to the AUI of the pulse transformer.

Output Load



Notes:

1. Load capacitance employed depends on output type:

   For 3SL, MOS, TPI, AUI: CL = 50 pF

   For 3SH, OCH: CL = 240 pF

2. Specifications which measure delays from an active state to a High-Z state are not guaranteed by production testing, but are characterized using 240 pF and are correlated to determine true driver turn-off time by eliminating inherent R-C delay times in measurements.

3. SW1 = Open for push-pull outputs during timing test.

   SW1 = V_{CC} for V_{OL} test.

   SW1 = GND for V_{OH} test.

   SW1 = V_{CC} for High-Z to active low and active low to High-Z measurements.

   SW1 = GND for High-Z to active high and active high to High-Z measurements.

Pin Capacitance

T_A = 25° C, f = 1 MHz

SYMBOL	PARAMETER	TYP	UNIT
C_{IN}	Input Capacitance	7	pF
C_{OUT}	Output Capacitance	10	pF

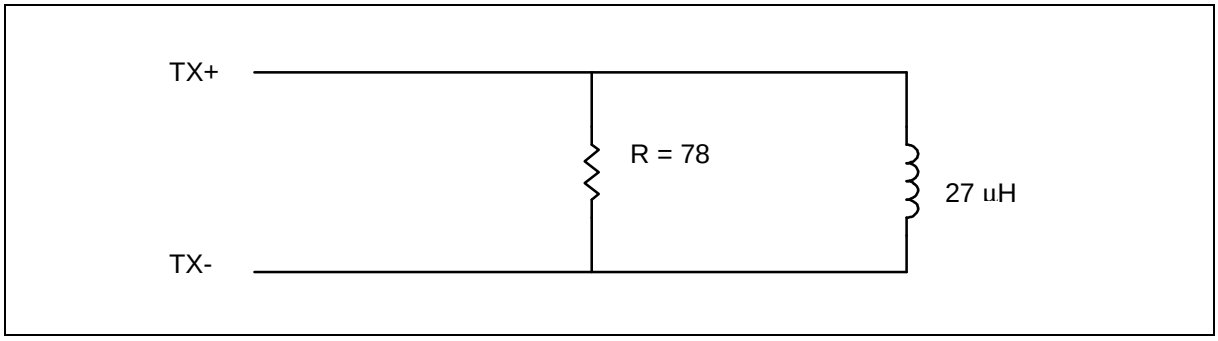
Derating Factor

Output timing is measured with a purely capacitive load of 50 pF or 240 pF. The following correction factor can be used for other loads (this factor is preliminary):

Derating for 3SL, MOS = -0.05 nS/pF

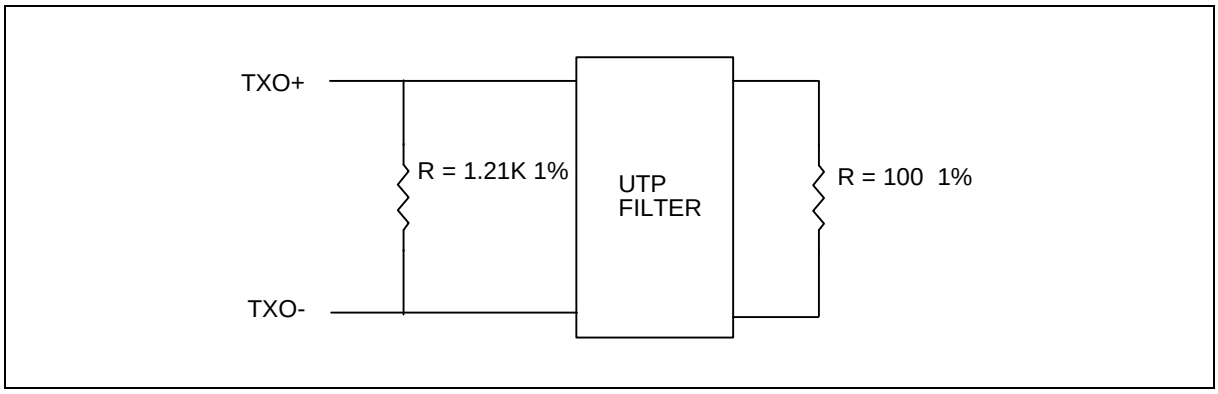
Derating for 3SH, OCL, TPI = -0.03 nS/pF

AUI Transmit Test Load



Note: In the above diagram, the TX+ and TX- signals are taken from the AUI side of the pulse transformer. The pulse transformer used for all testing is a 100µH +/-0.1% Pulse Engineering PE64103.

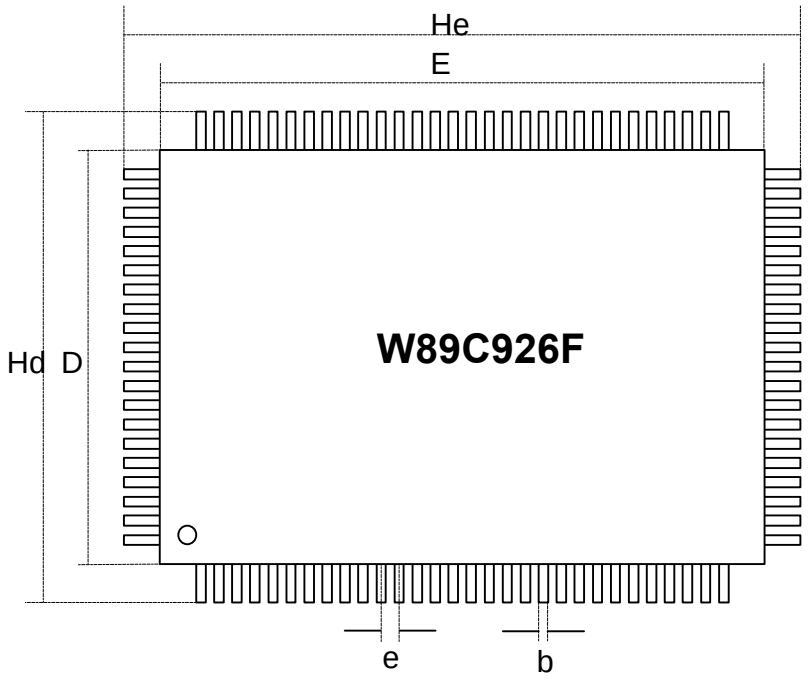
UTP Transmit Test Load

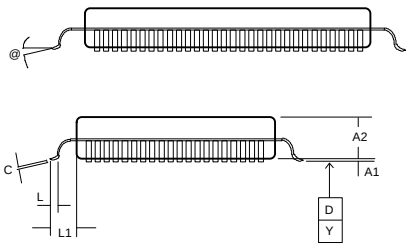


Note: In the above diagram, the UTP filter used for all testing is a Valor FL1012.

PACKAGE DIMENSIONS

The PENTIC+ is packaged in a 100-pin TQFP for type II PC card applications. Detailed dimensions are shown below.





Symbol	Dimensions in inches	Dimensions in mm
A1	0.004 +/- 0.002	0.10 +/- 0.05
A2	0.055 +/- 0.002	1.40 +/- 0.05
b	0.013 + 0.002 - 0.004	0.32 + 0.06 - 0.10
C	0.008 max 0.004 min	0.20 max 0.09 min
D	0.551 ± 0.004	14.00 ± 0.10
E	0.787 ± 0.004	20.00 ± 0.10
e	0.026 typ	0.65 typ
Hd	0.630 ± 0.004	16.00 ± 0.10
He	0.866 ± 0.004	22.00 ± 0.10
L	0.024 ± 0.006	0.60 ± 0.15
L1	0.039 typ	1.00 typ
Y	0.003 max	0.08 max
@	0 to 7	0 to 7

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